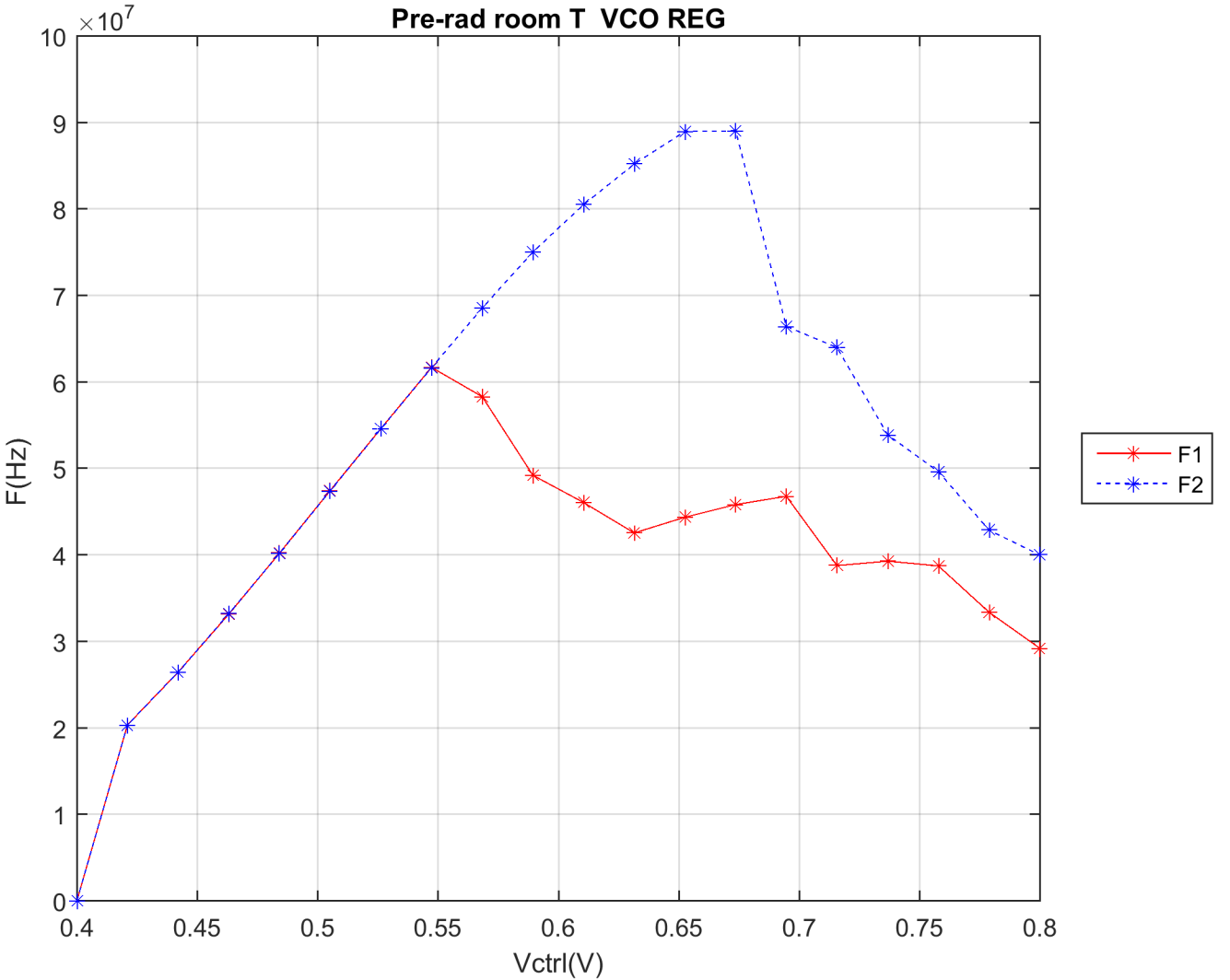
EXPERIMENT: 200Mrads cold (-20C):

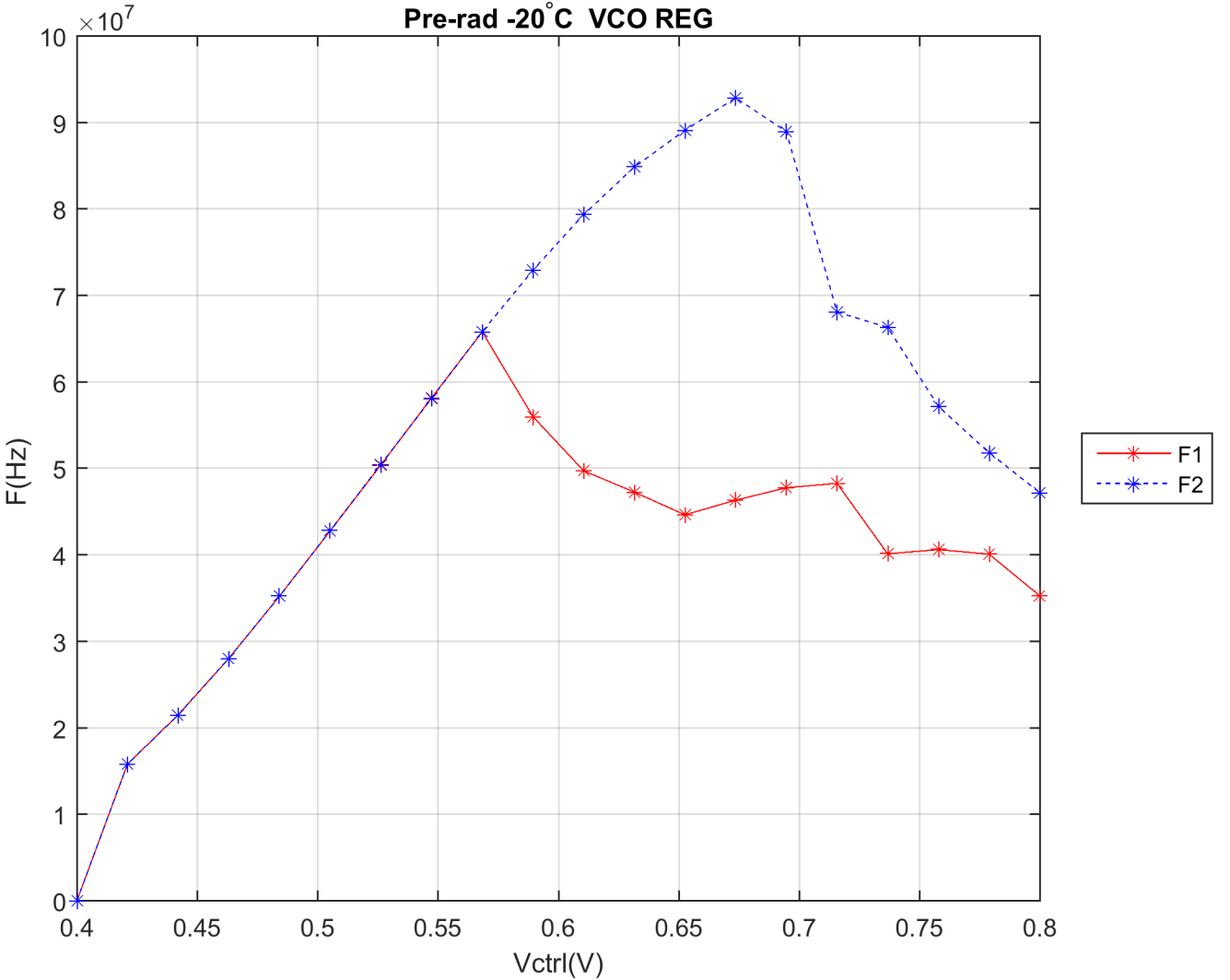
OVERVIEW:
1st. Irradiation at -20C, up to 200Mrads.
2nd. Room temperature annealing for one month.
3rd. High temperature annealing, 60C, 20 days. Measurements were taken at 60C.
4th. High temperature annealing, 100C, 2 days. Measurements taken at 100C.

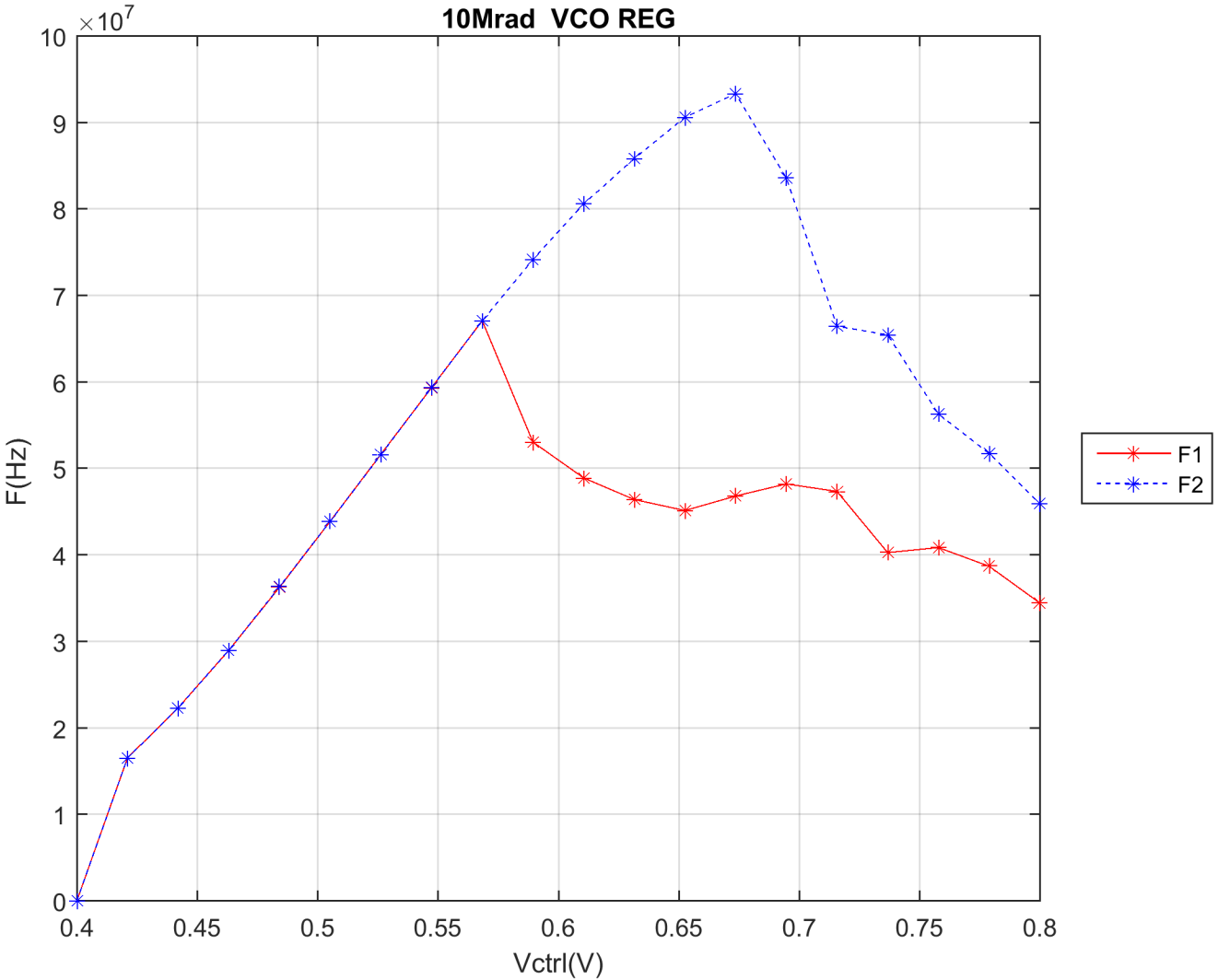
Results of three tests are included, reapeted for several TID and in different time stamps during annealing:
1. Vctrl sweep for REG transistors VCO (measuring the frequency vs Vctrl).
2. Vctrl sweep for ELT transistors VCO (measuring the frequency vs Vctrl).
3. Skip test for ELT transistor VCO.The voltage used for the VCO (Vctrl) in the skip test depends on the results obtained in 2:it uses the voltage needed in 2 to reach around 50MHz (the software reads the results of the previous test and it takes the Vctrl that makes the VCO oscillate with the closest frequency to 50MHz but always below 50MHz).

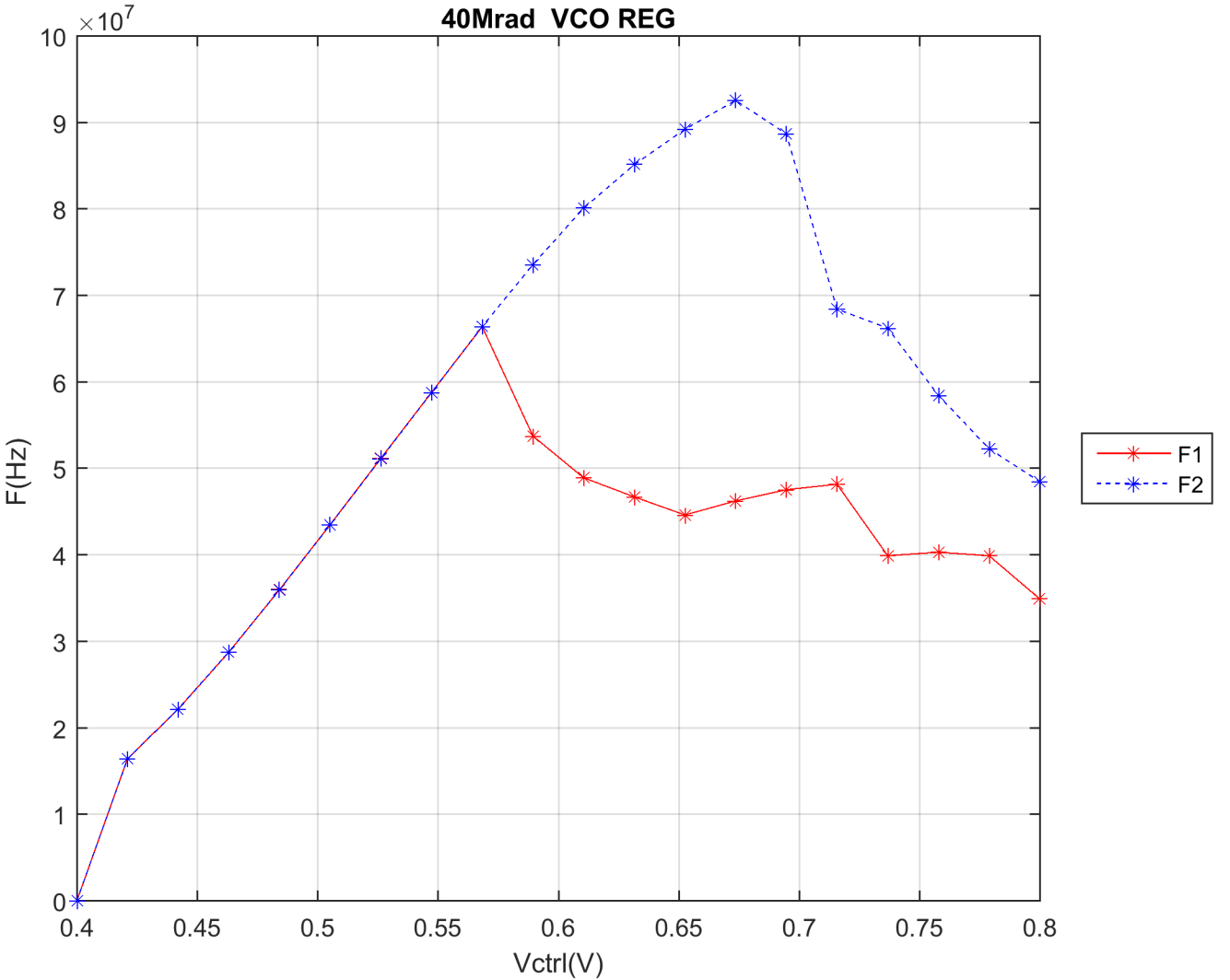
(More data is available for other TIDs, here only some of the points are shown).

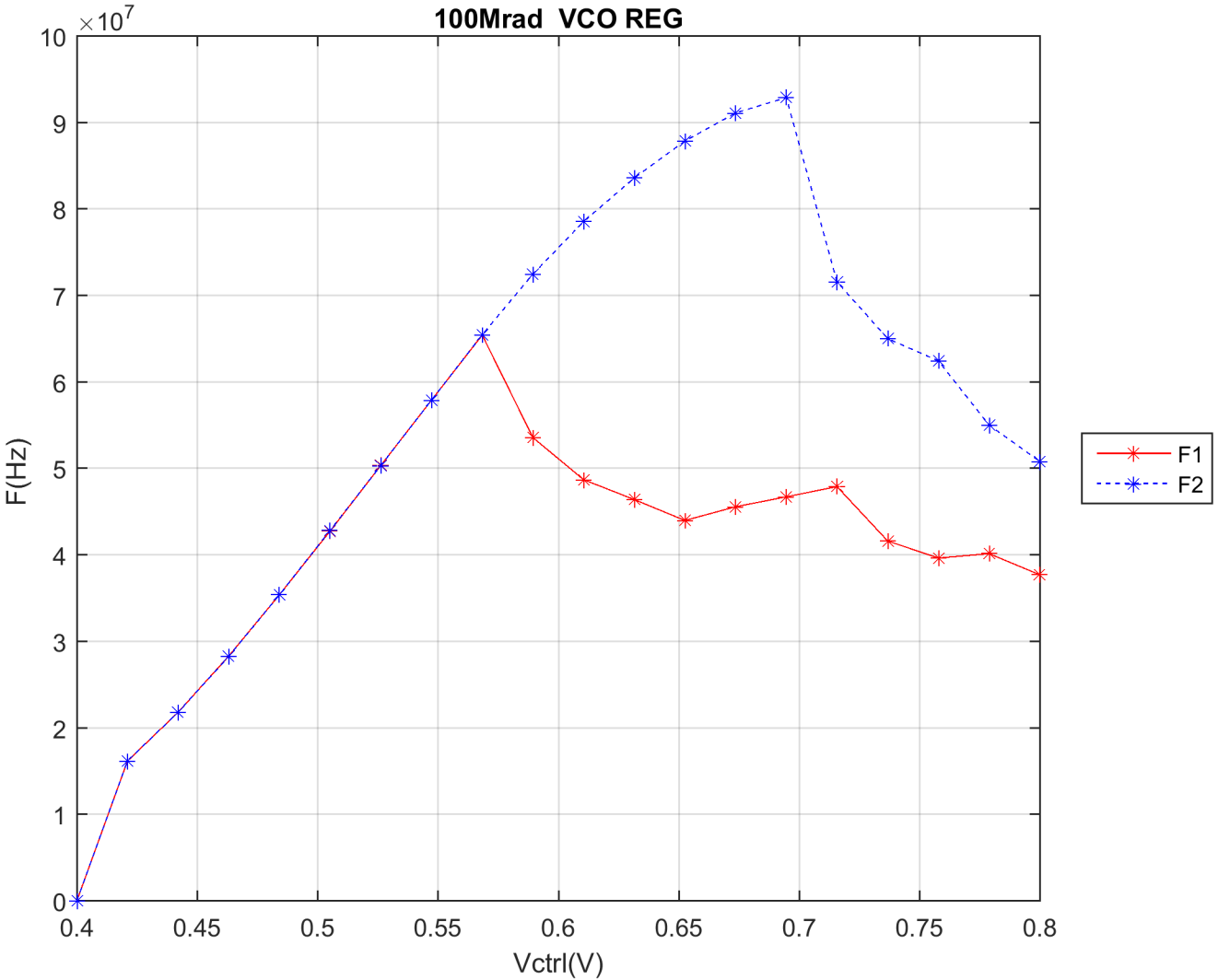
1. Vctrl sweep for REG transistors VCO (measuring the frequency vs Vctrl).

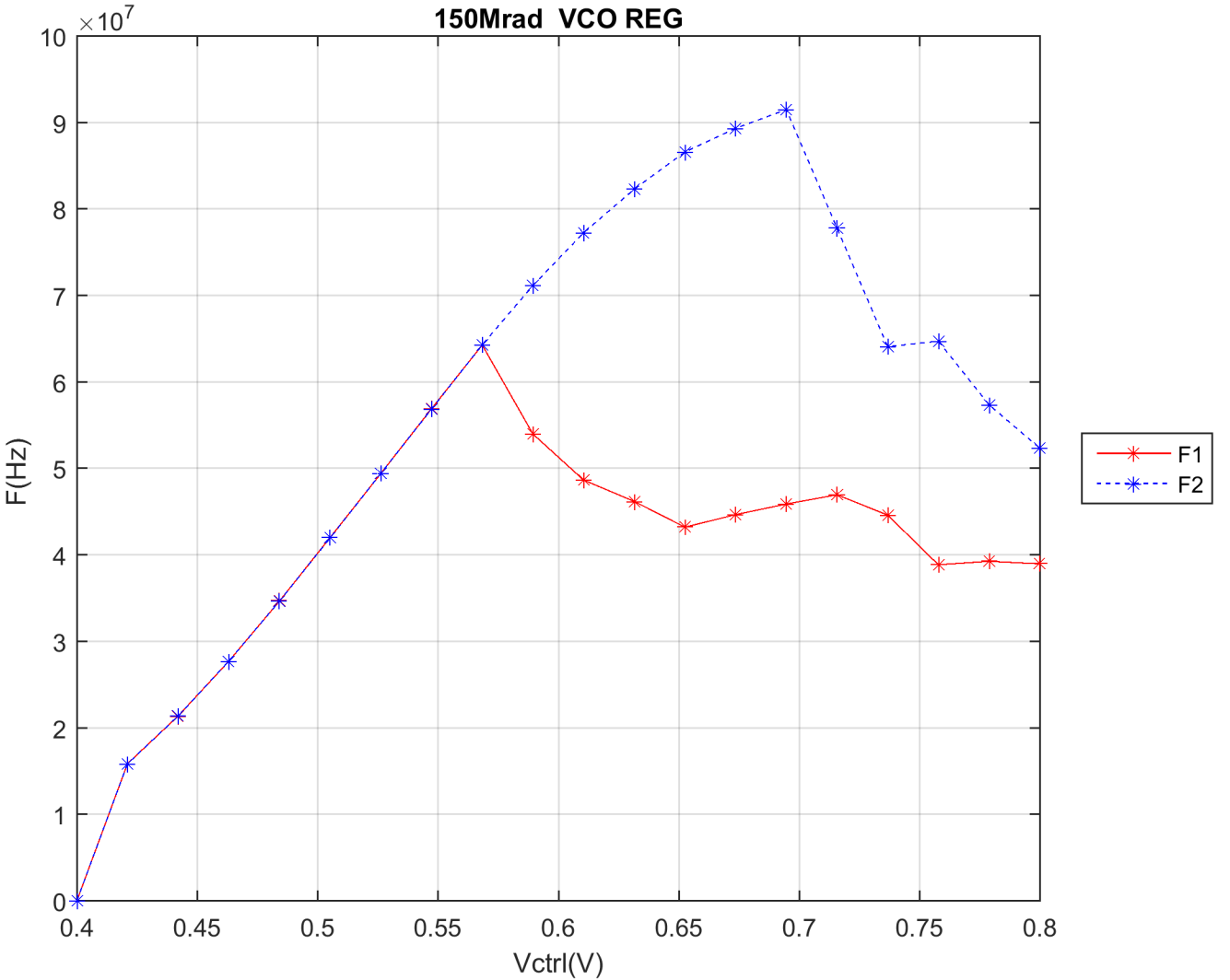

Pre-rad room T VCO REG
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

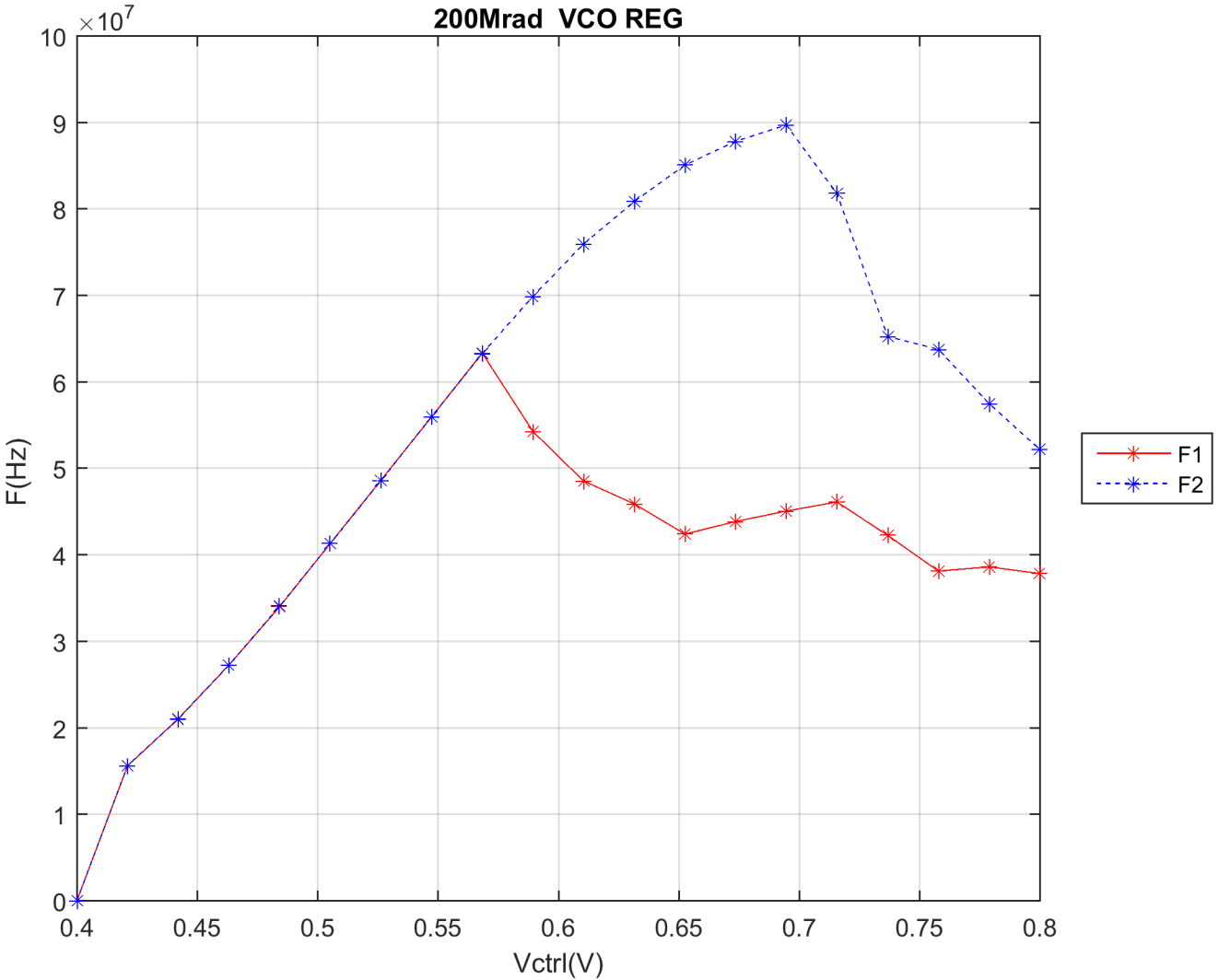

Pre-rad -20°C VCO REG
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

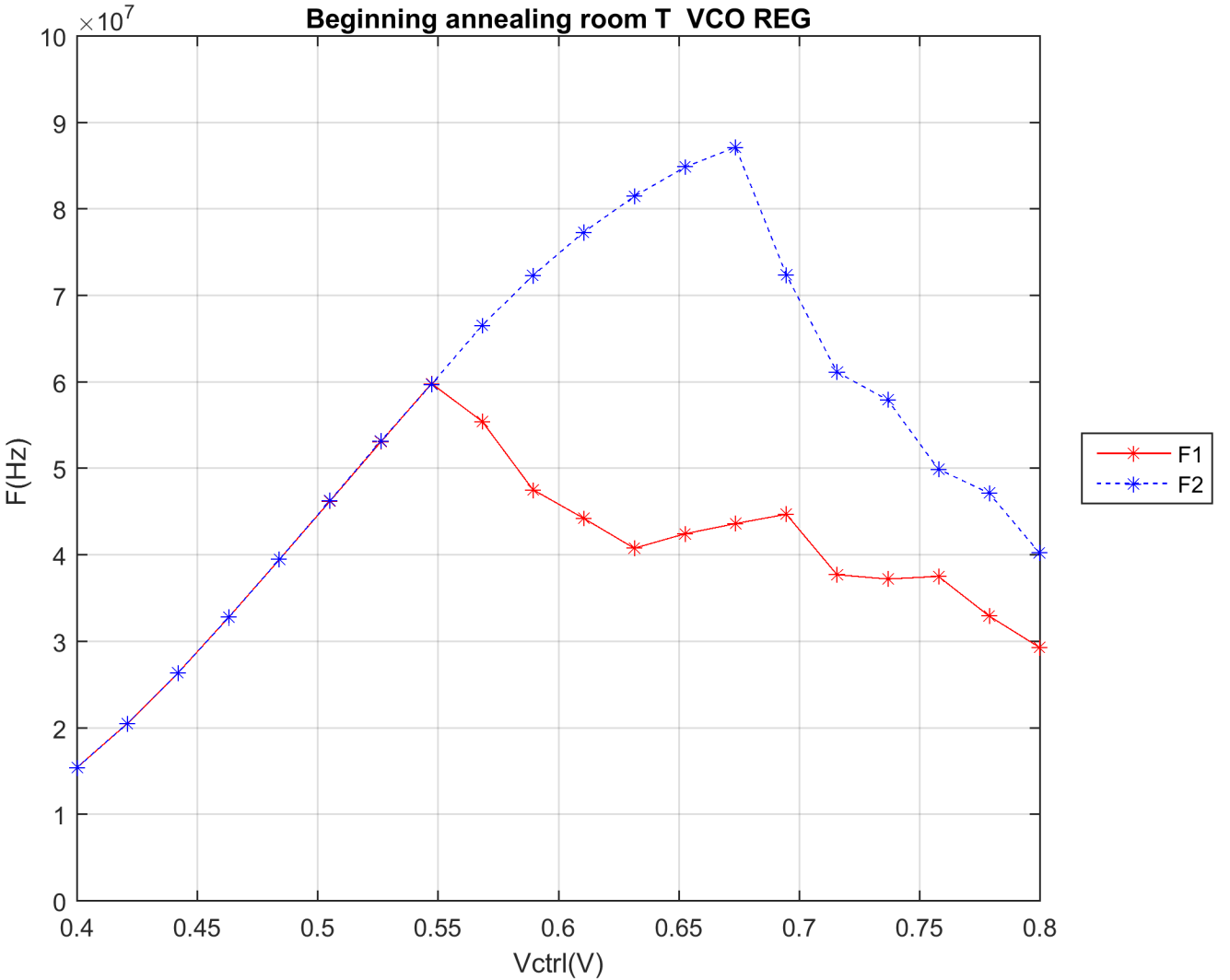

10Mrad VCO REG
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

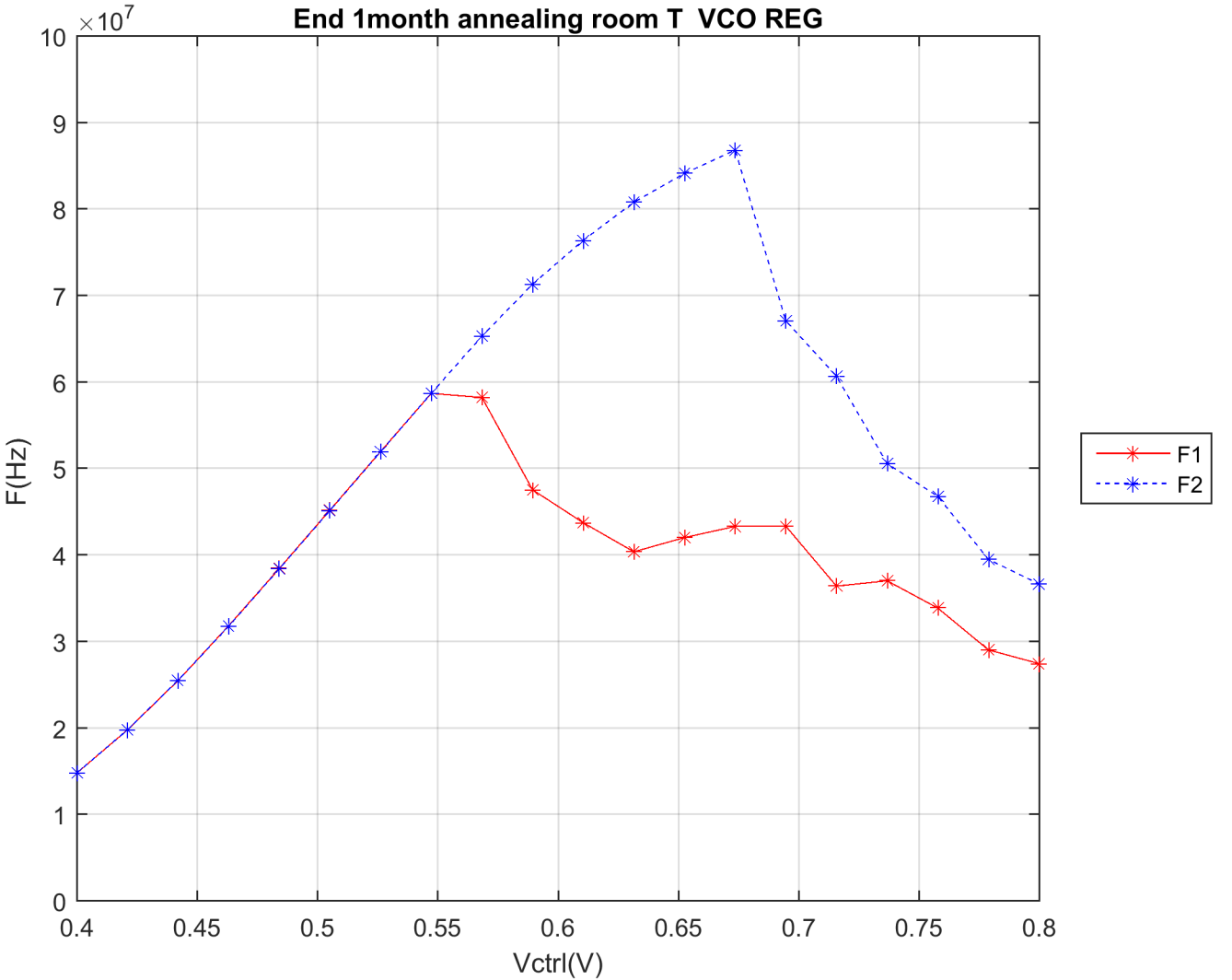

40Mrad VCO REG
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

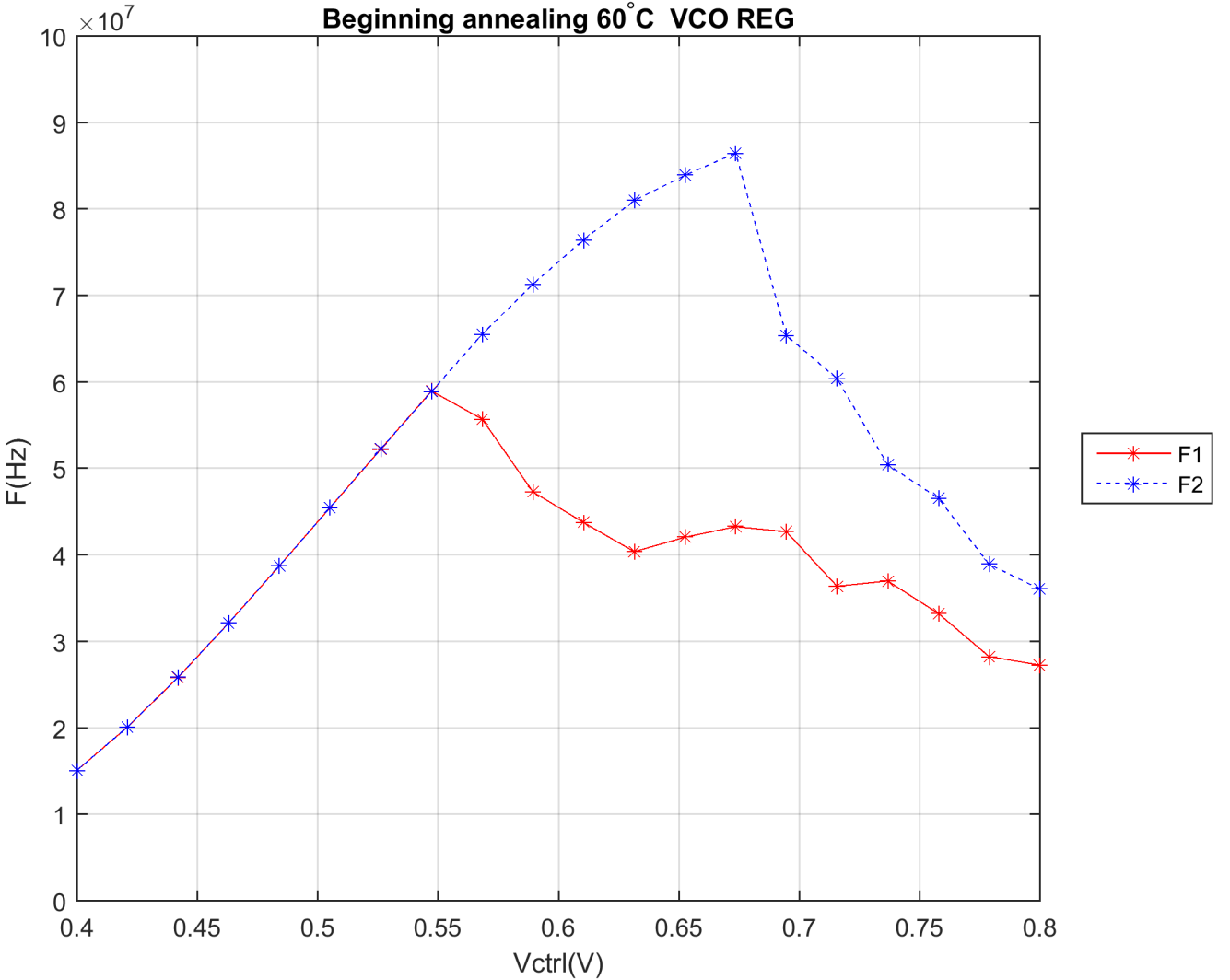

100Mrad VCO REG
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

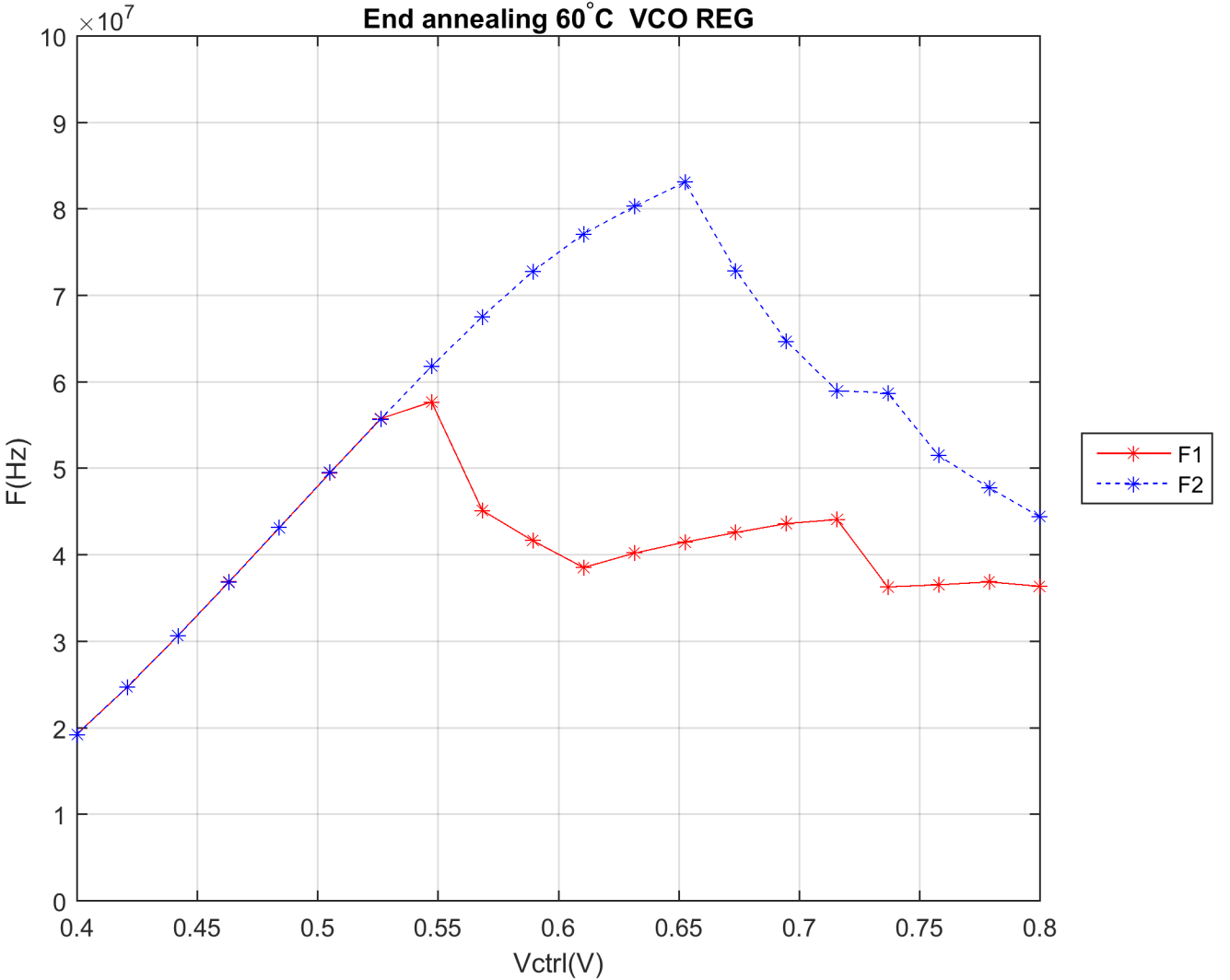

150Mrad VCO REG
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

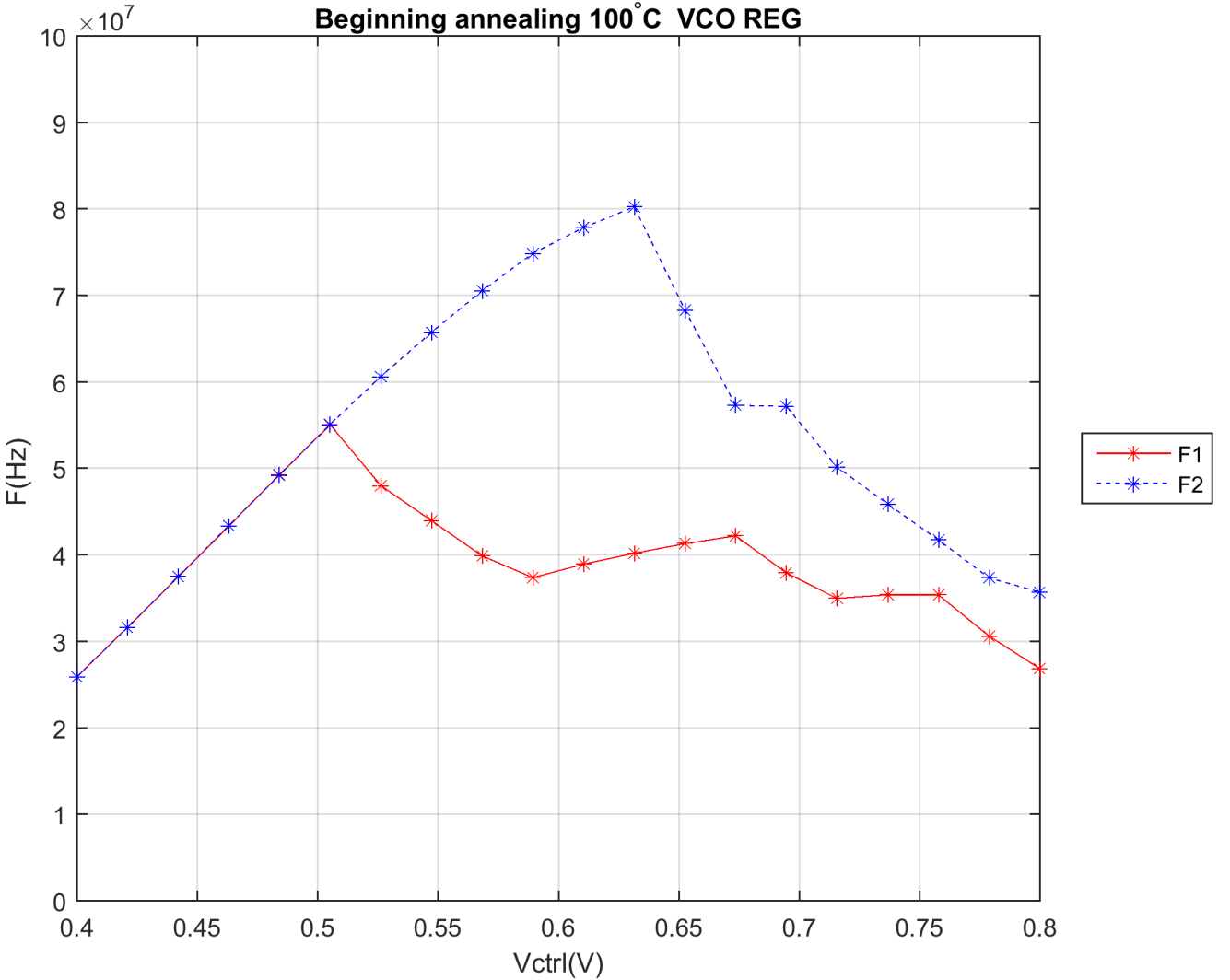

200Mrad VCO REG
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

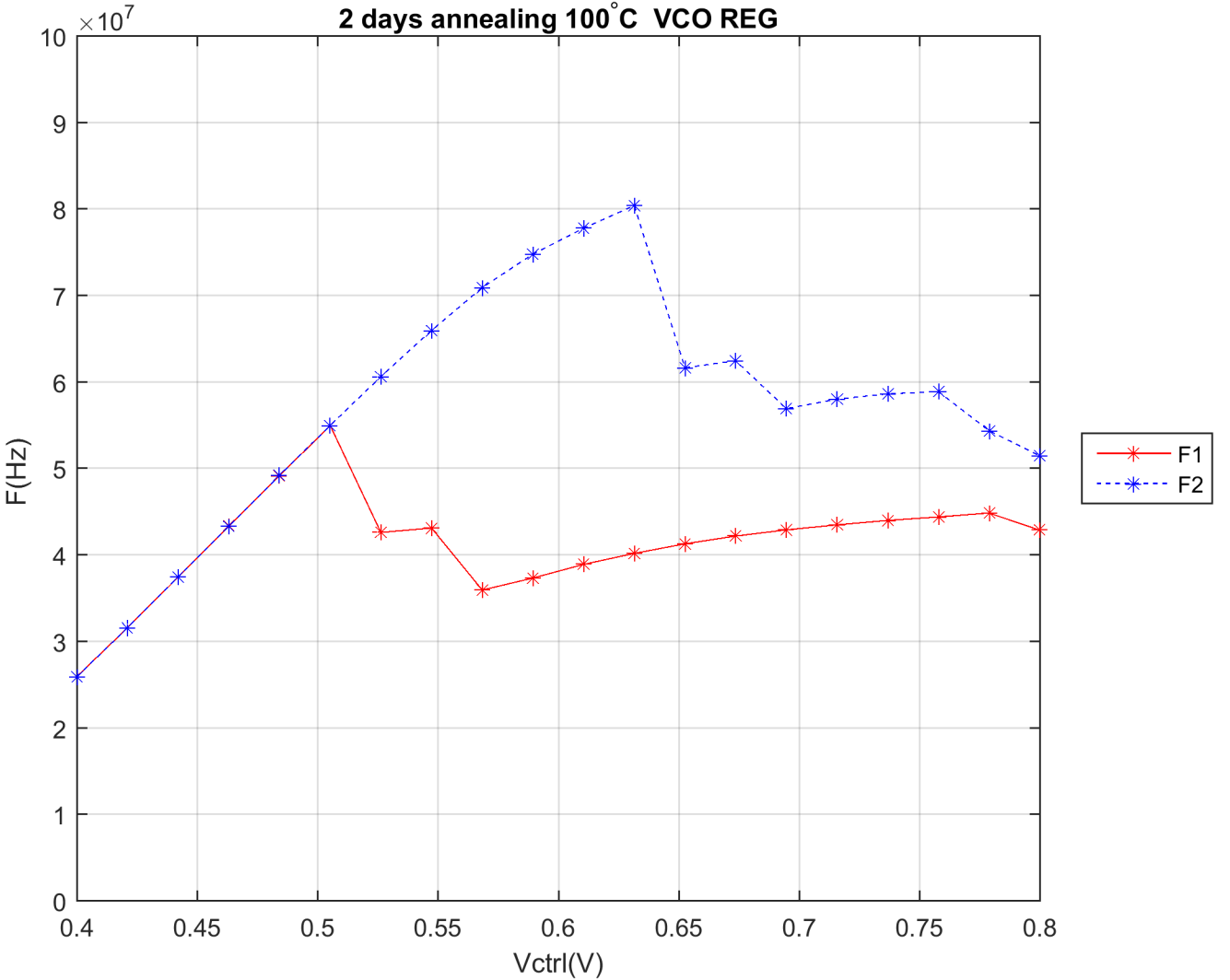

Beginning annealing room T VCO REG
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2


End 1month annealing room T VCO REG
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

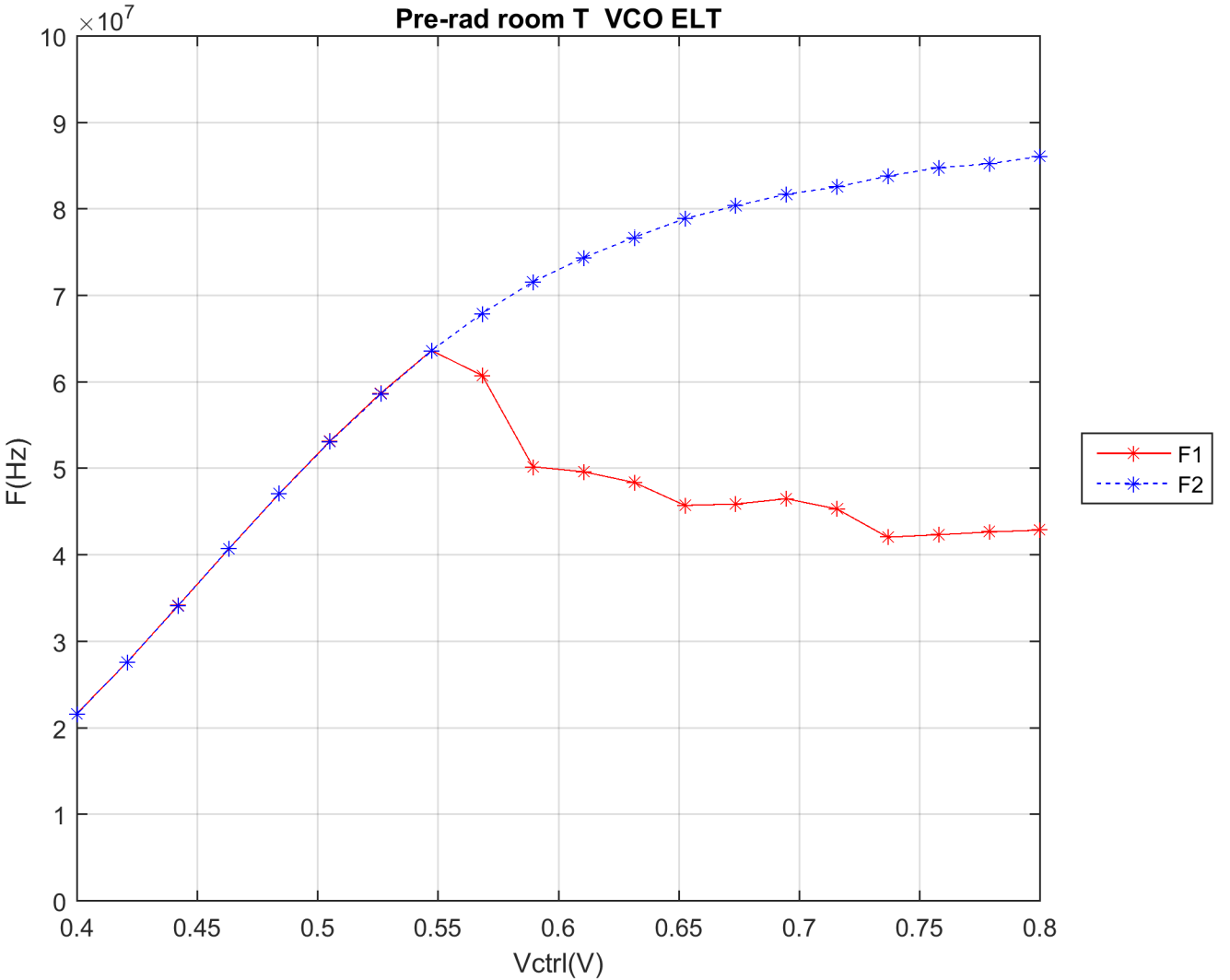

Beginning annealing 60°C VCO REG
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

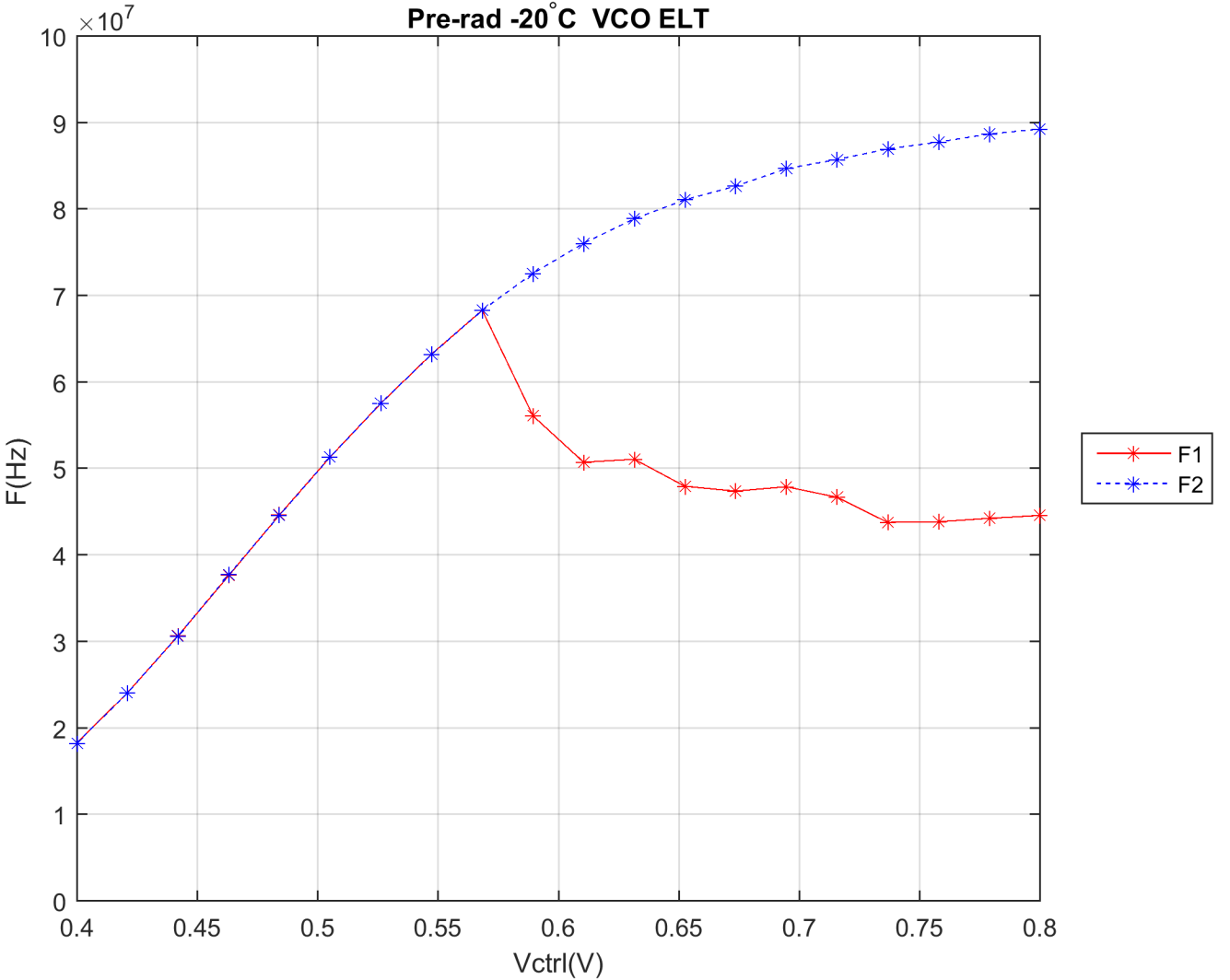

End annealing 60°C VCO REG
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

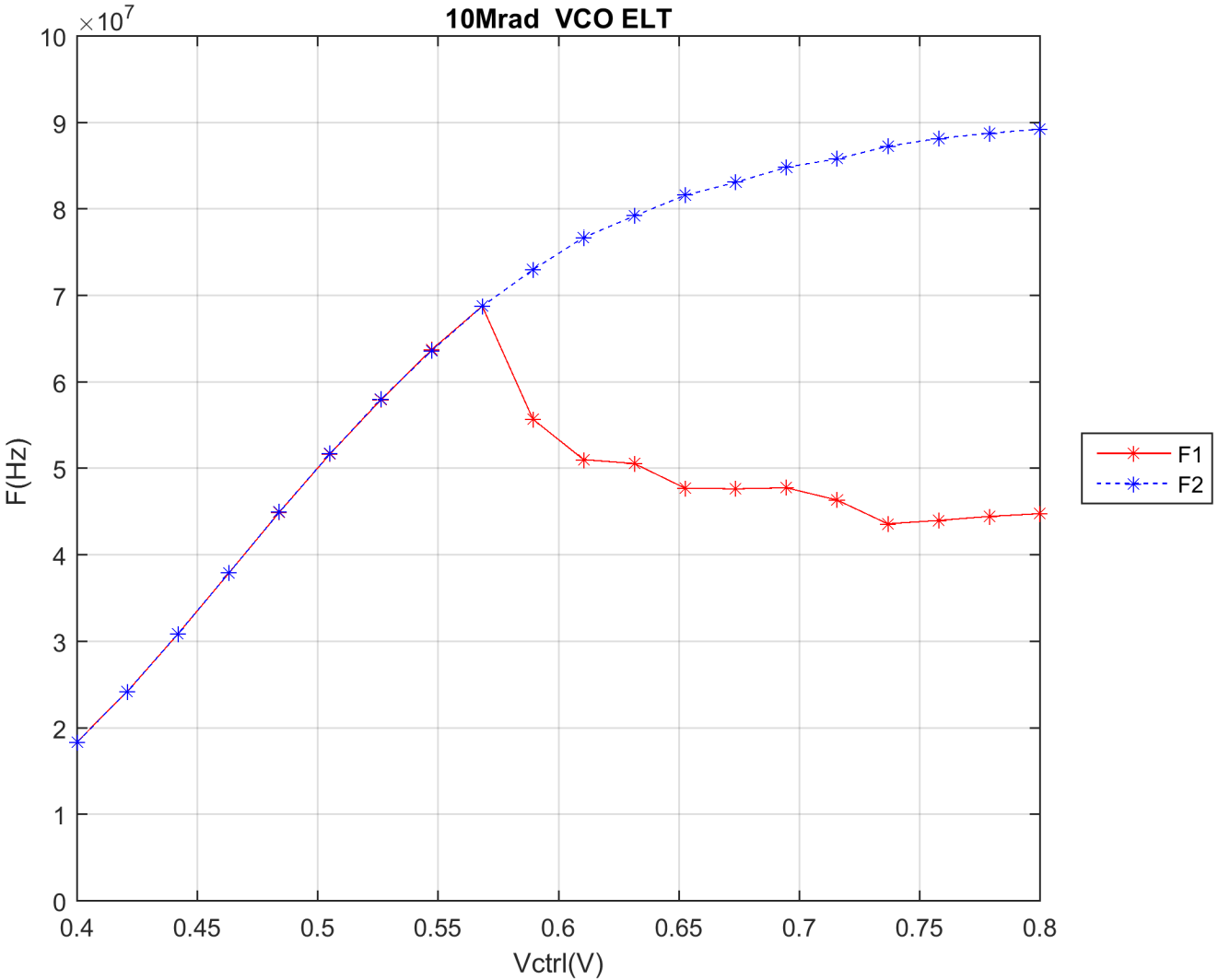

Beginning annealing 100°C VCO REG
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

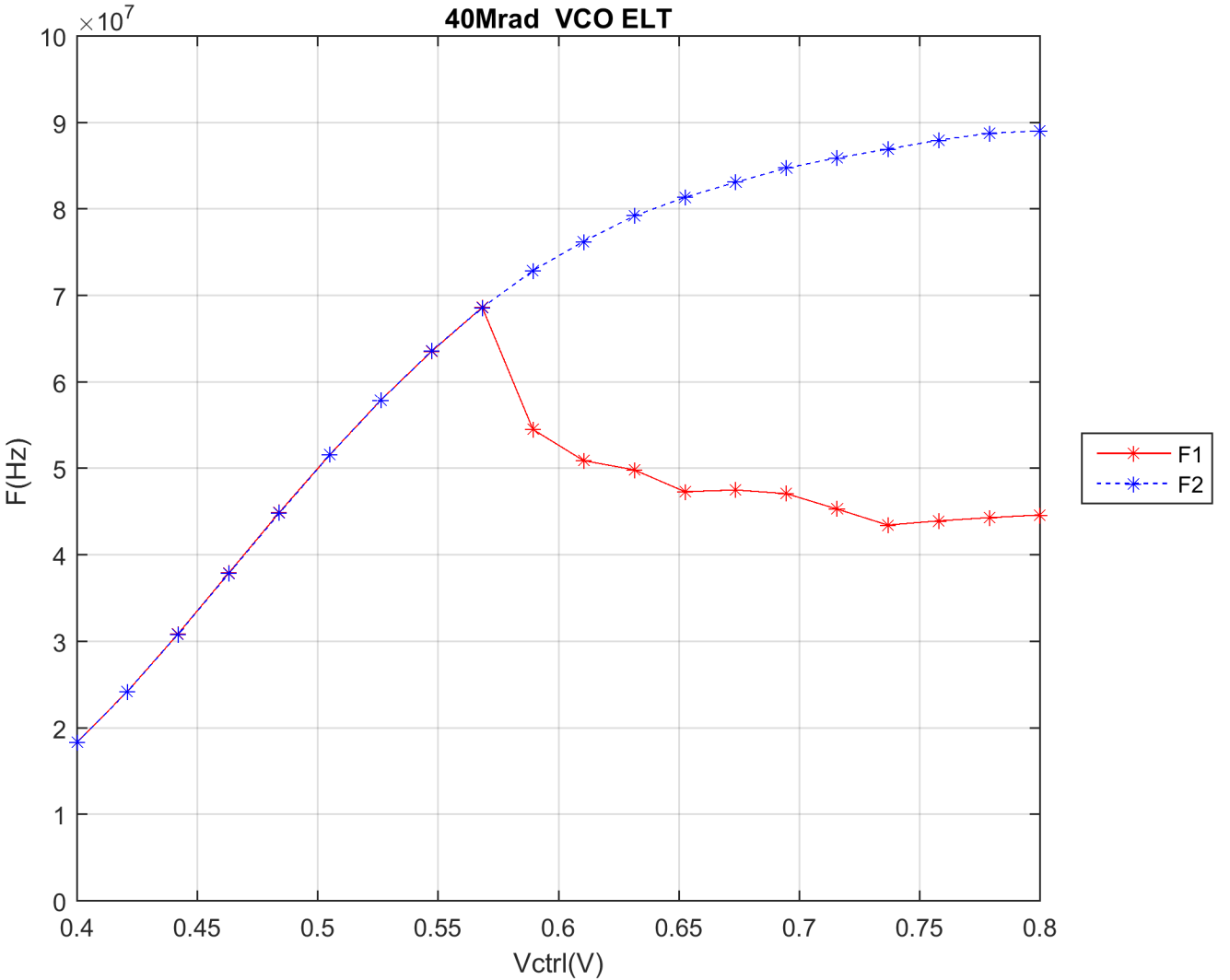

2 days annealing 100°C VCO REG
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

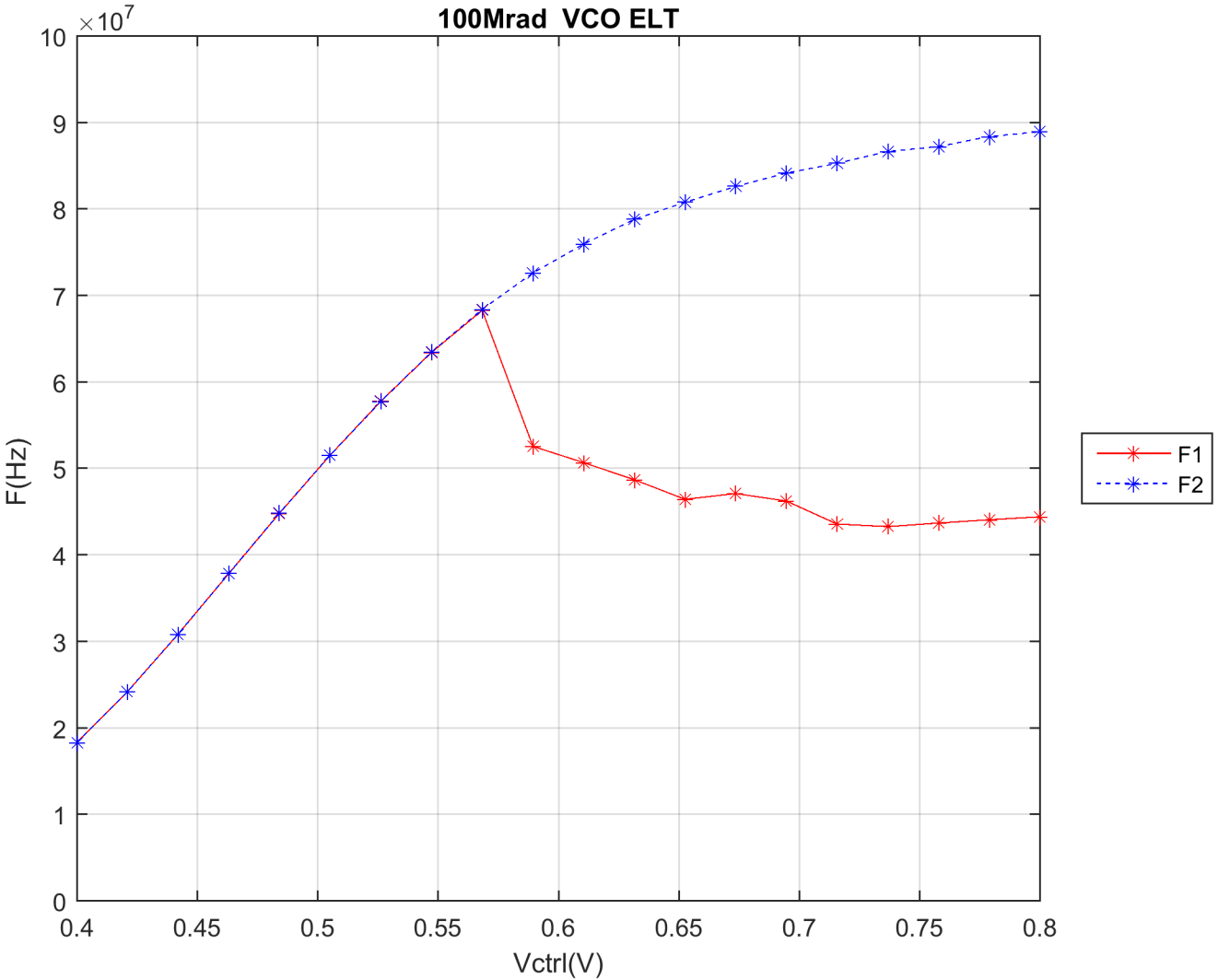
2. Vctrl sweep for ELT transistors VCO (measuring the frequency vs Vctrl).

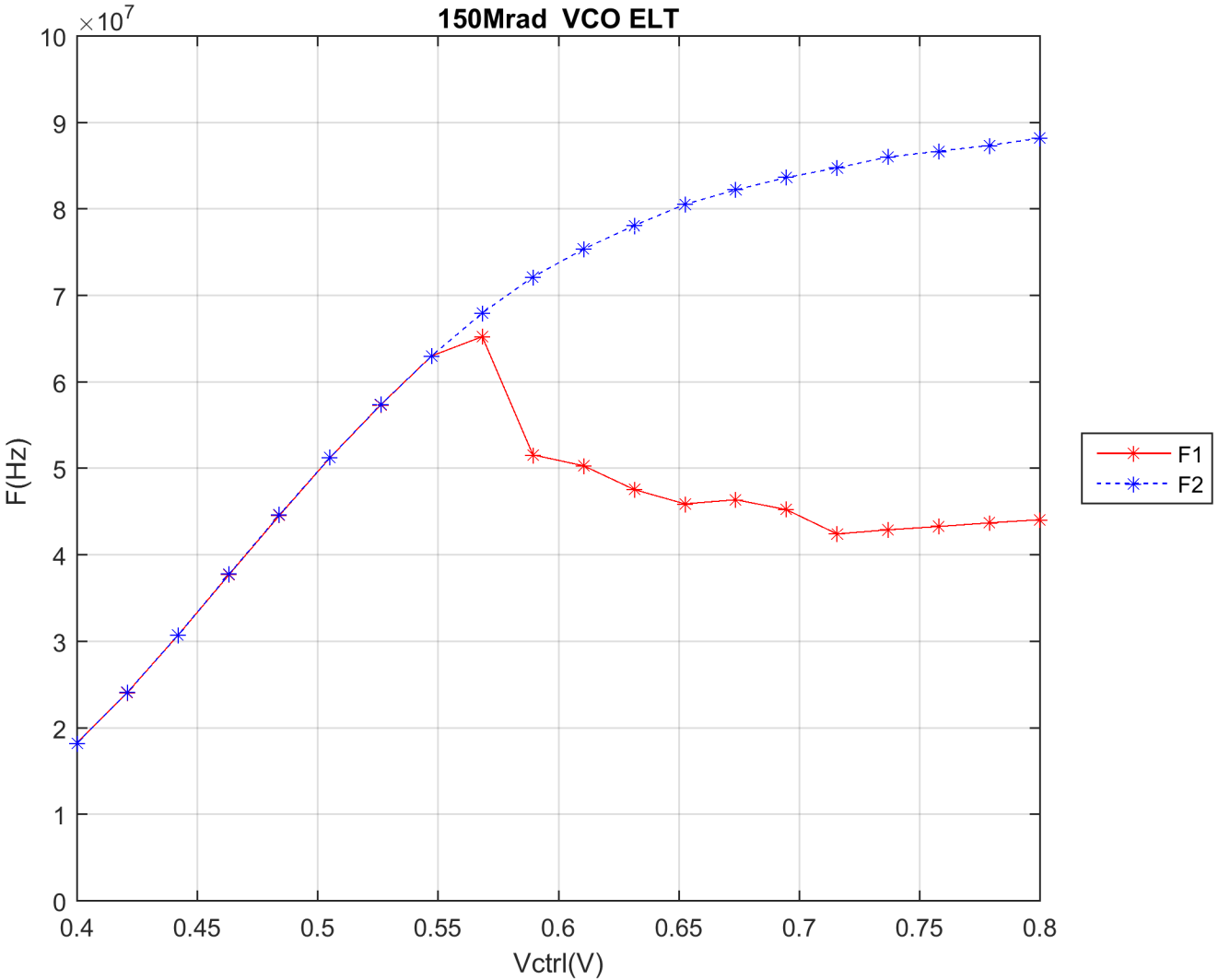

Pre-rad room T VCO ELT
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

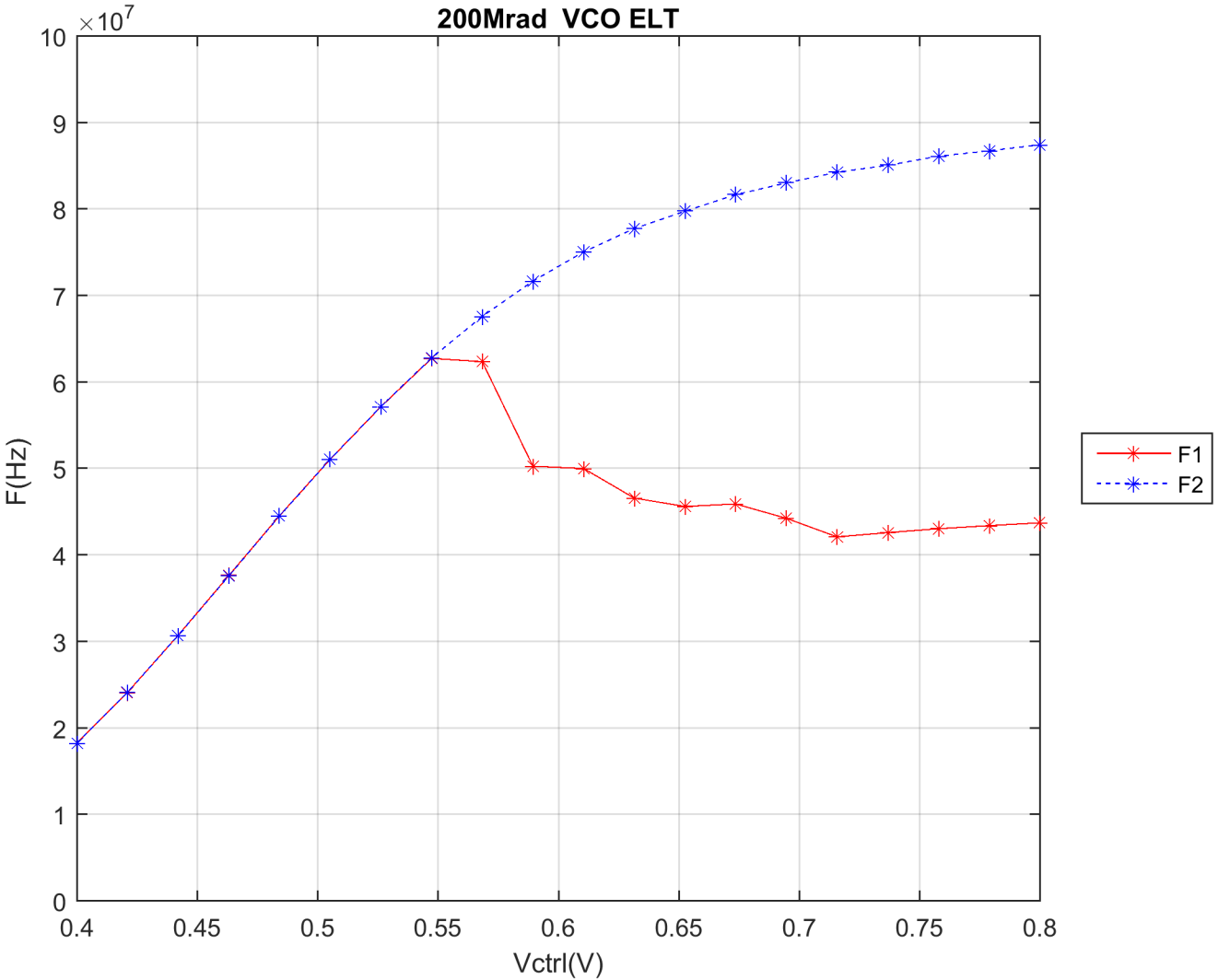

Pre-rad -20°C VCO ELT
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

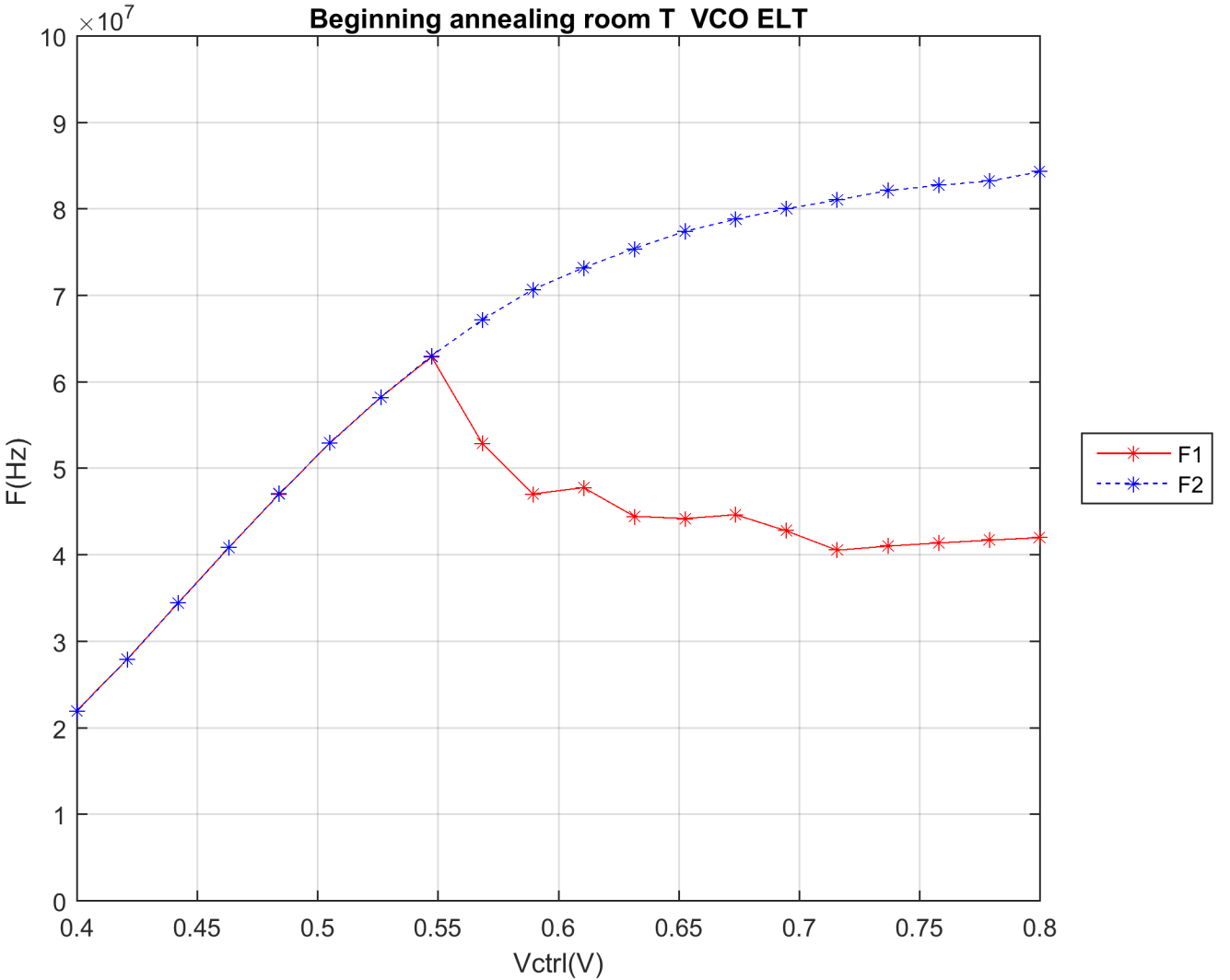

10Mrad VCO ELT
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

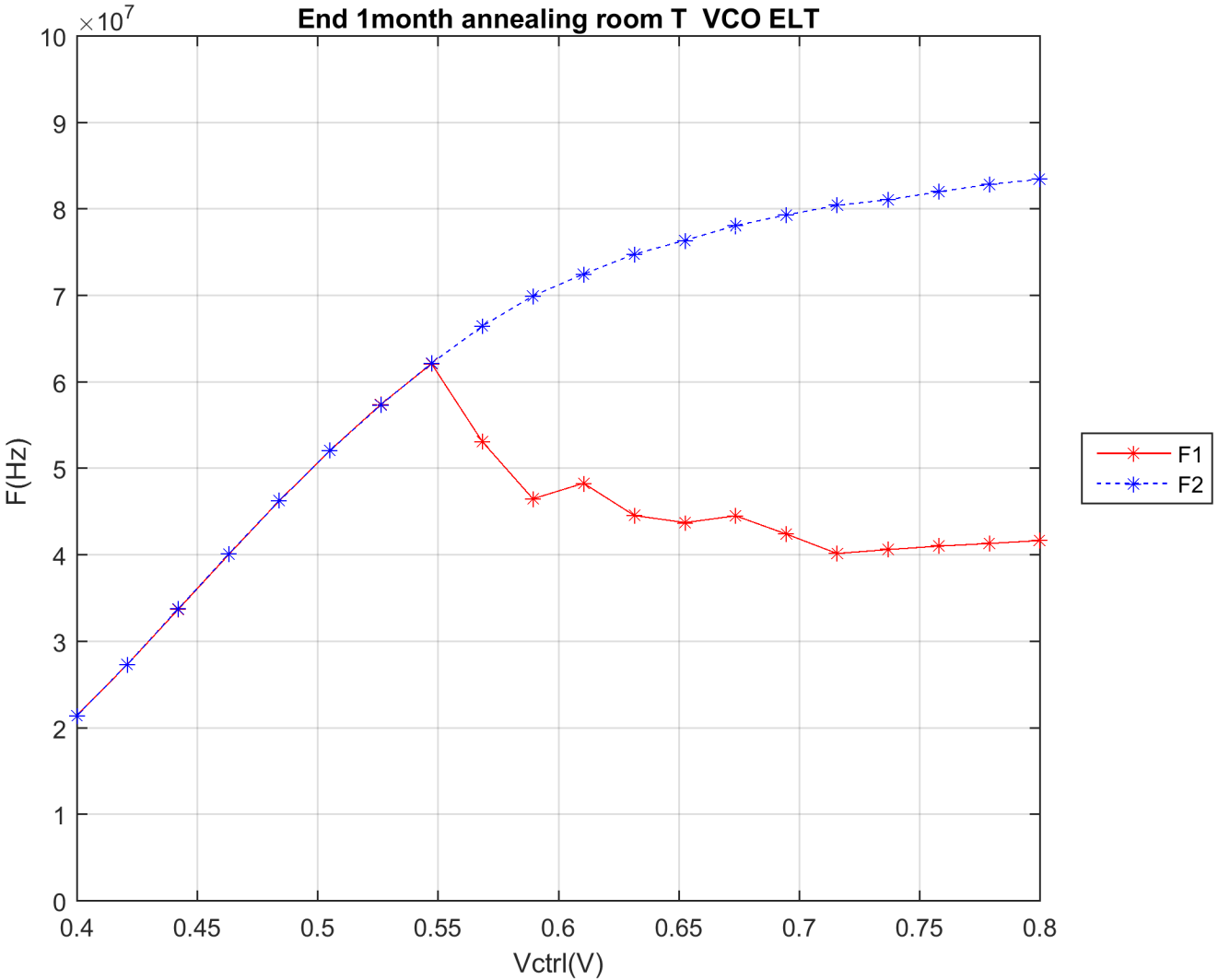

40Mrad VCO ELT
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

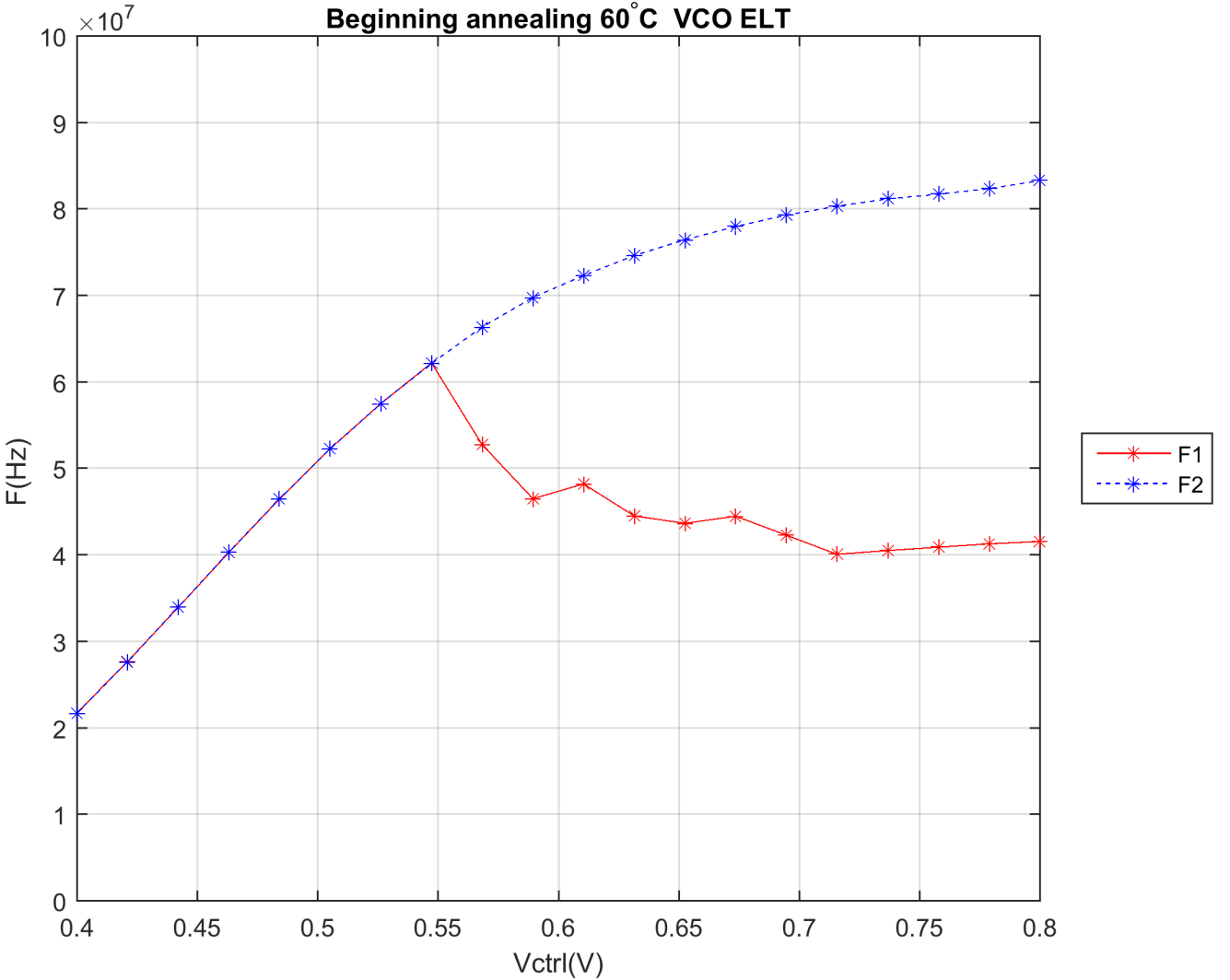

100Mrad VCO ELT
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

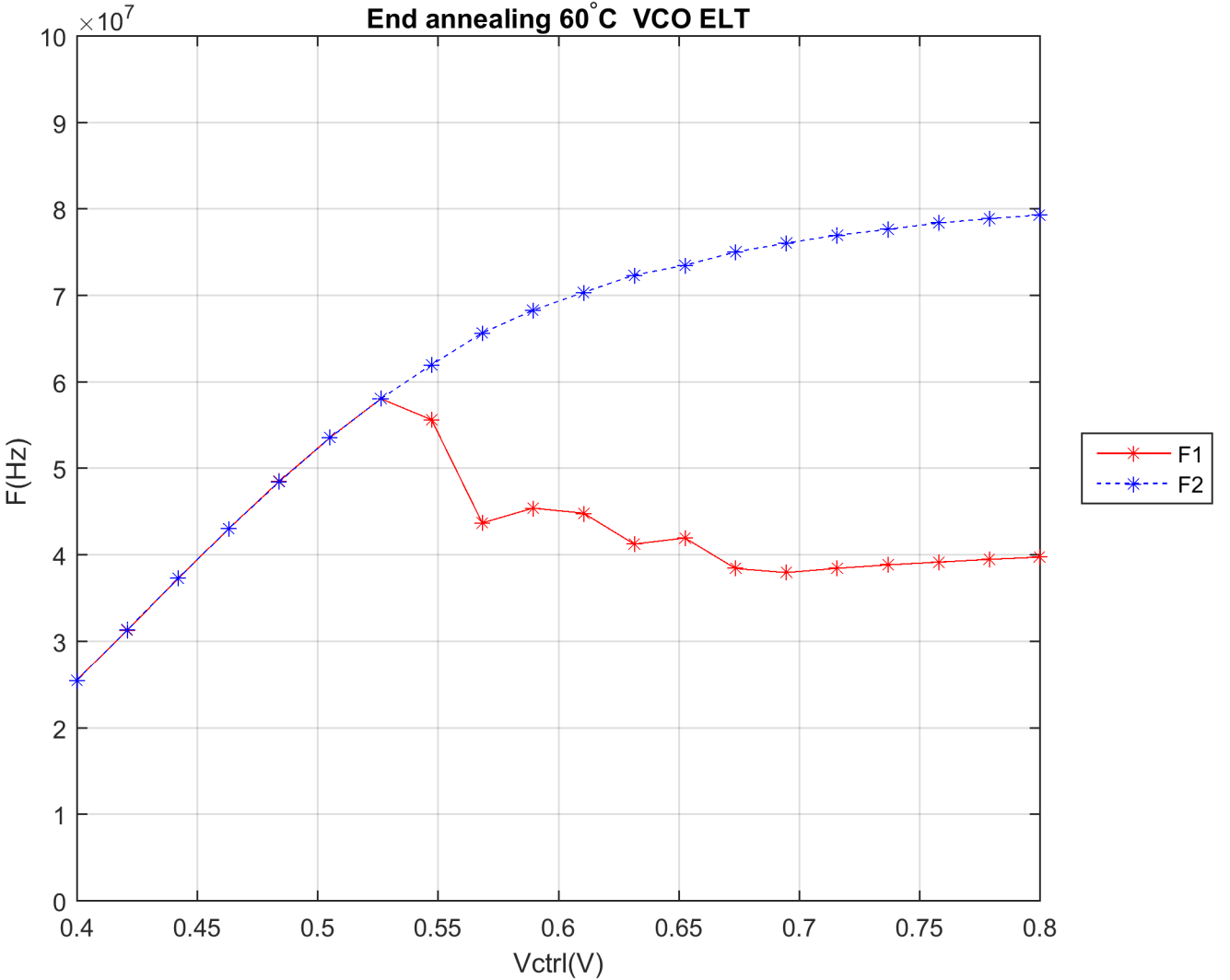

150Mrad VCO ELT
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

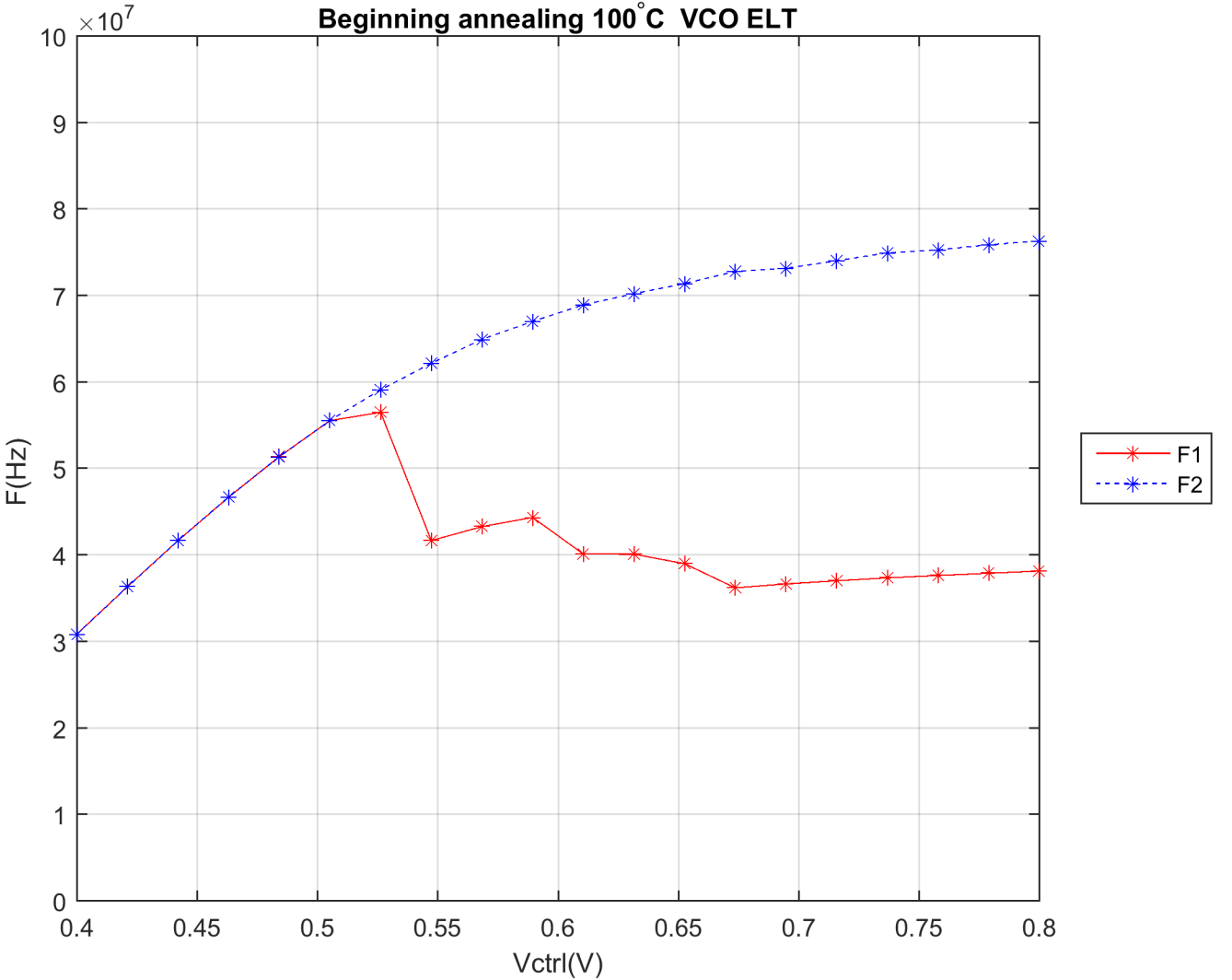

200Mrad VCO ELT
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

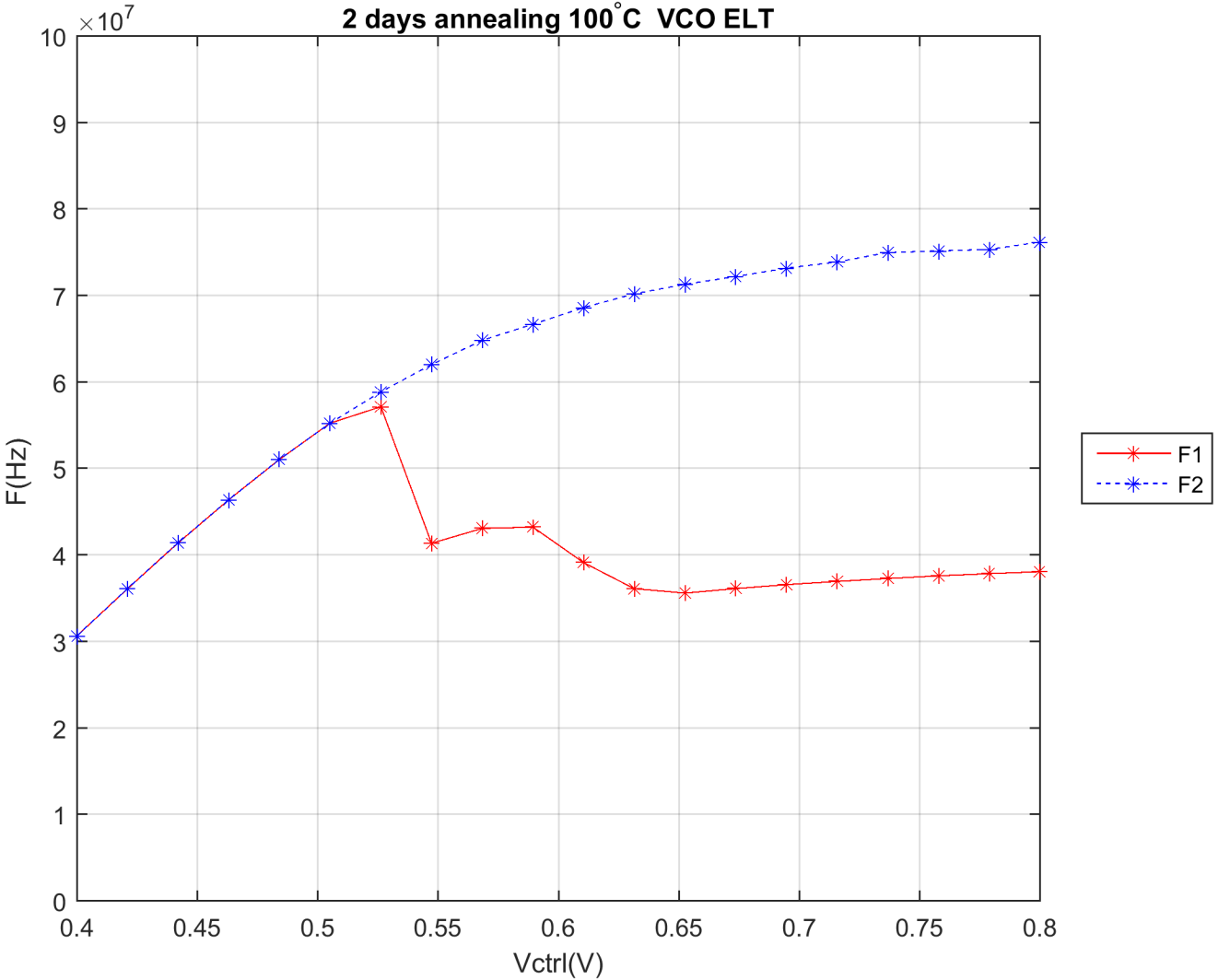

Beginning annealing room T VCO ELT
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2


End 1month annealing room T VCO ELT
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

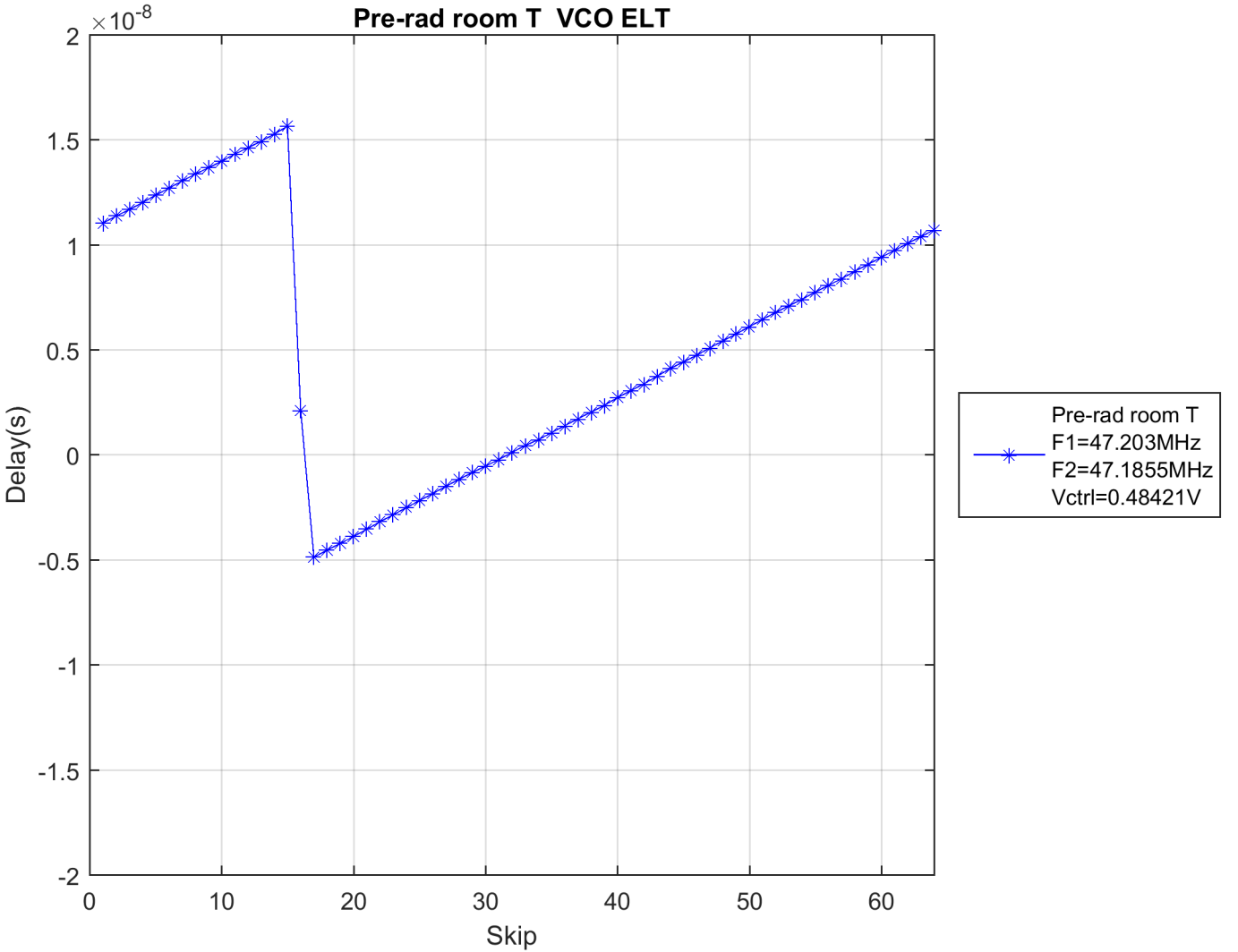

Beginning annealing 60°C VCO ELT
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

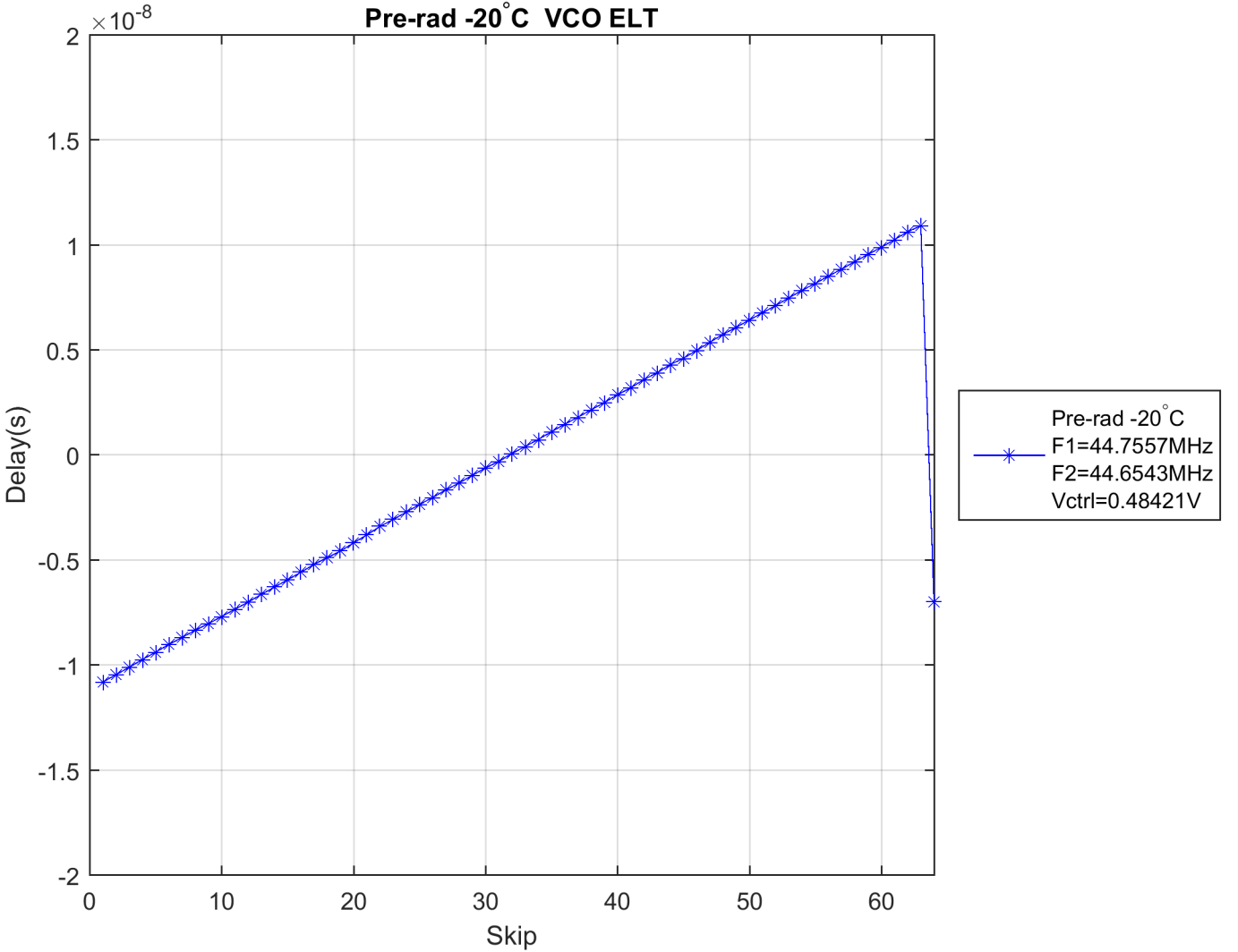

End annealing 60°C VCO ELT
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

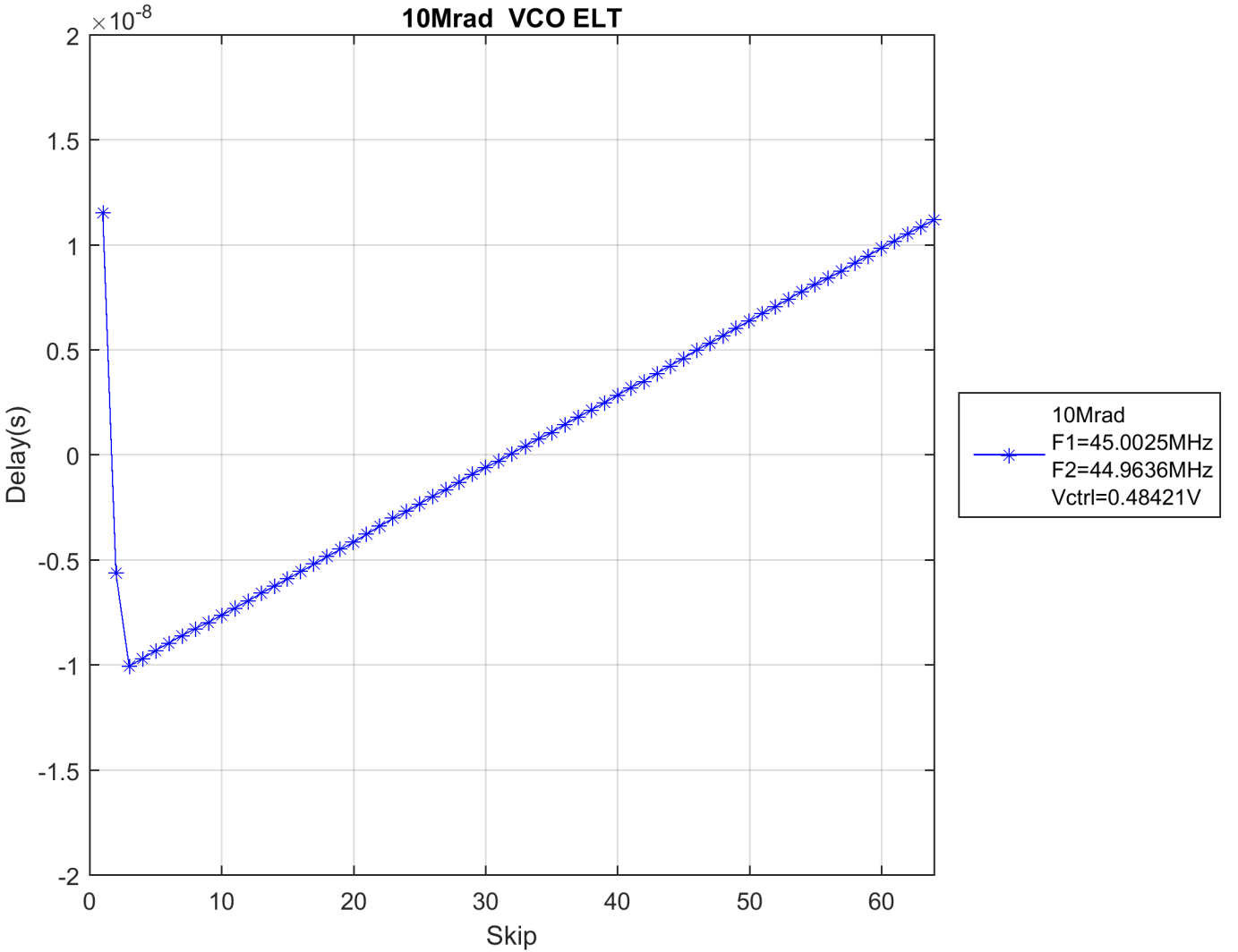

Beginning annealing 100°C VCO ELT
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

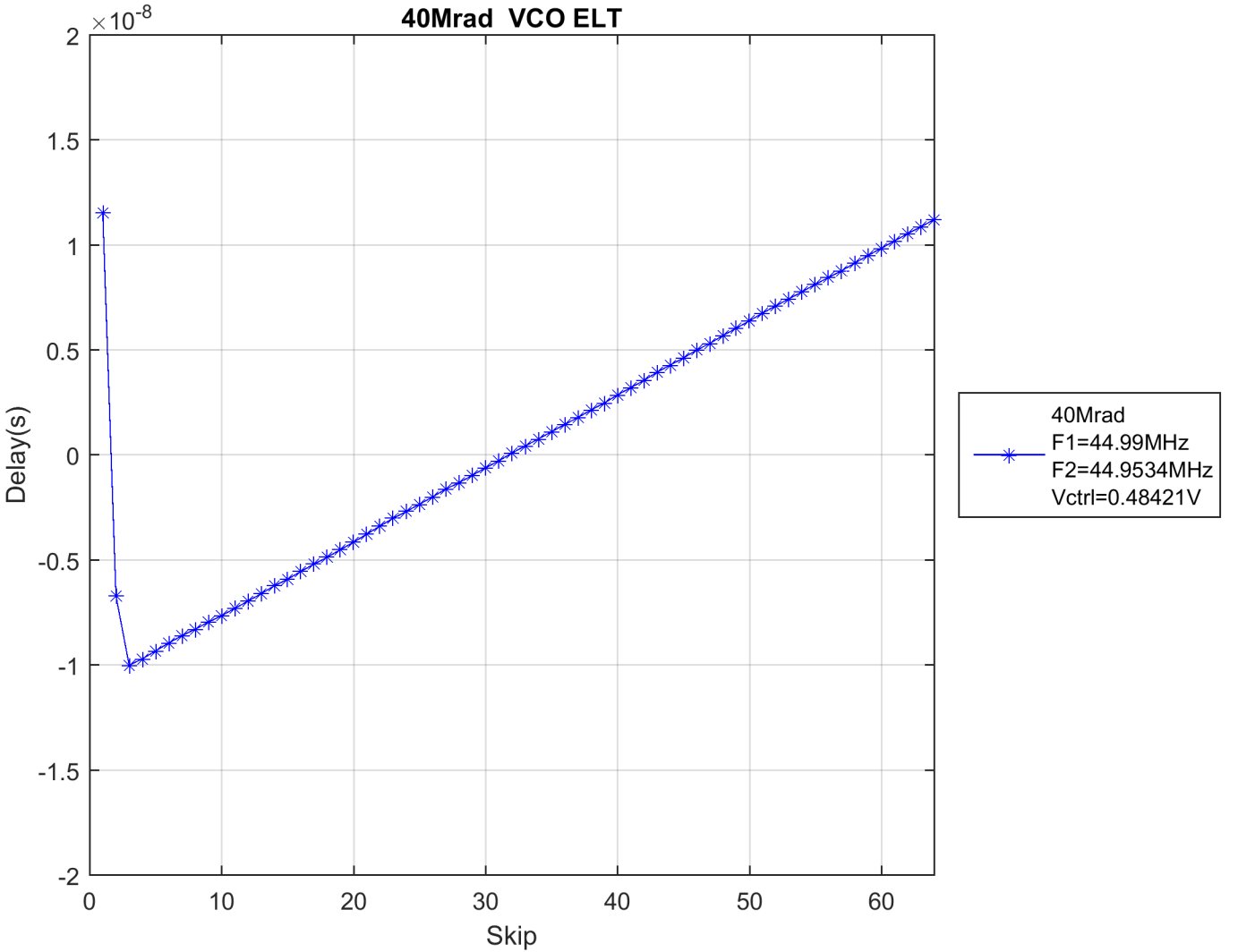

2 days annealing 100°C VCO ELT
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

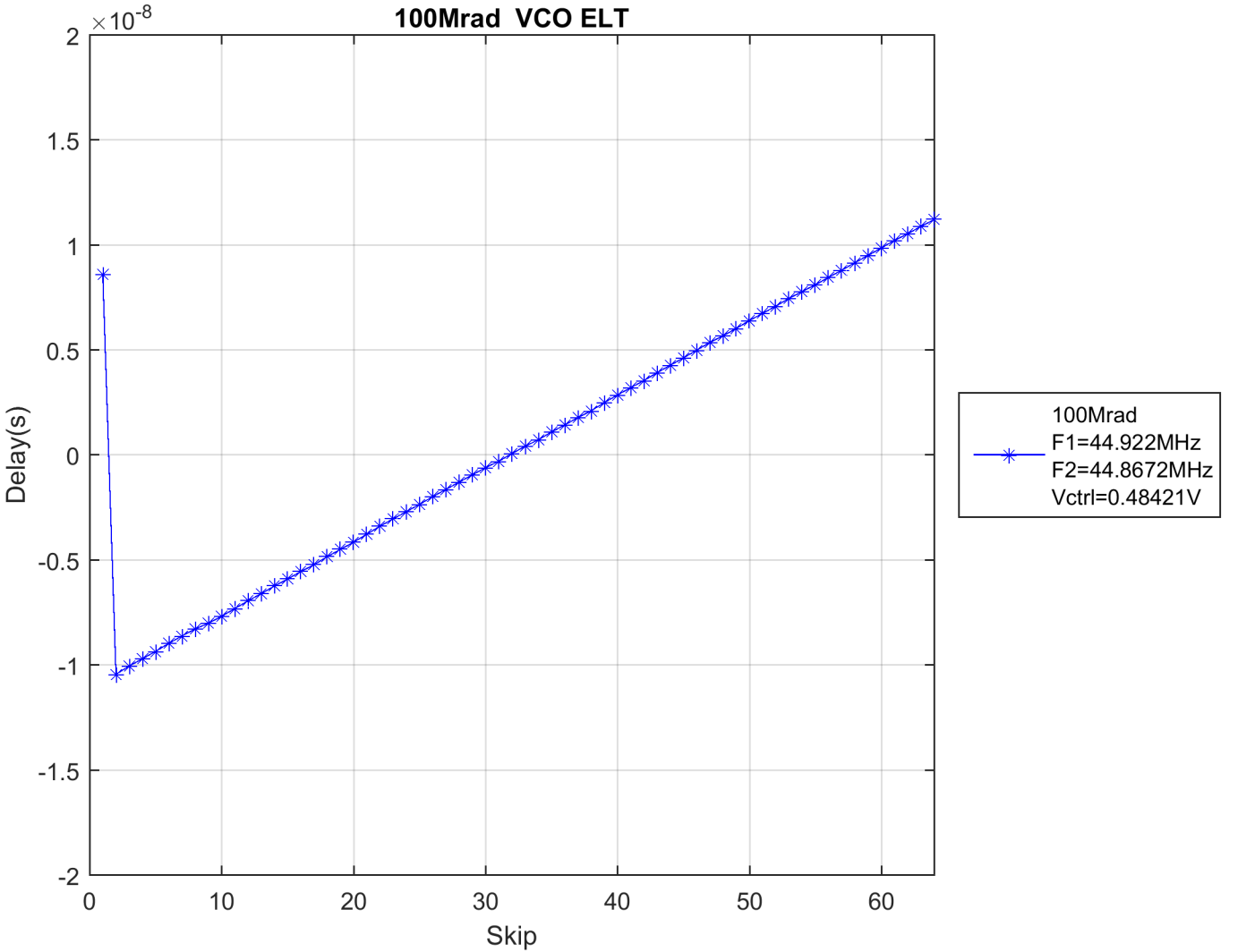
3. Skip test for ELT transistor VCO.

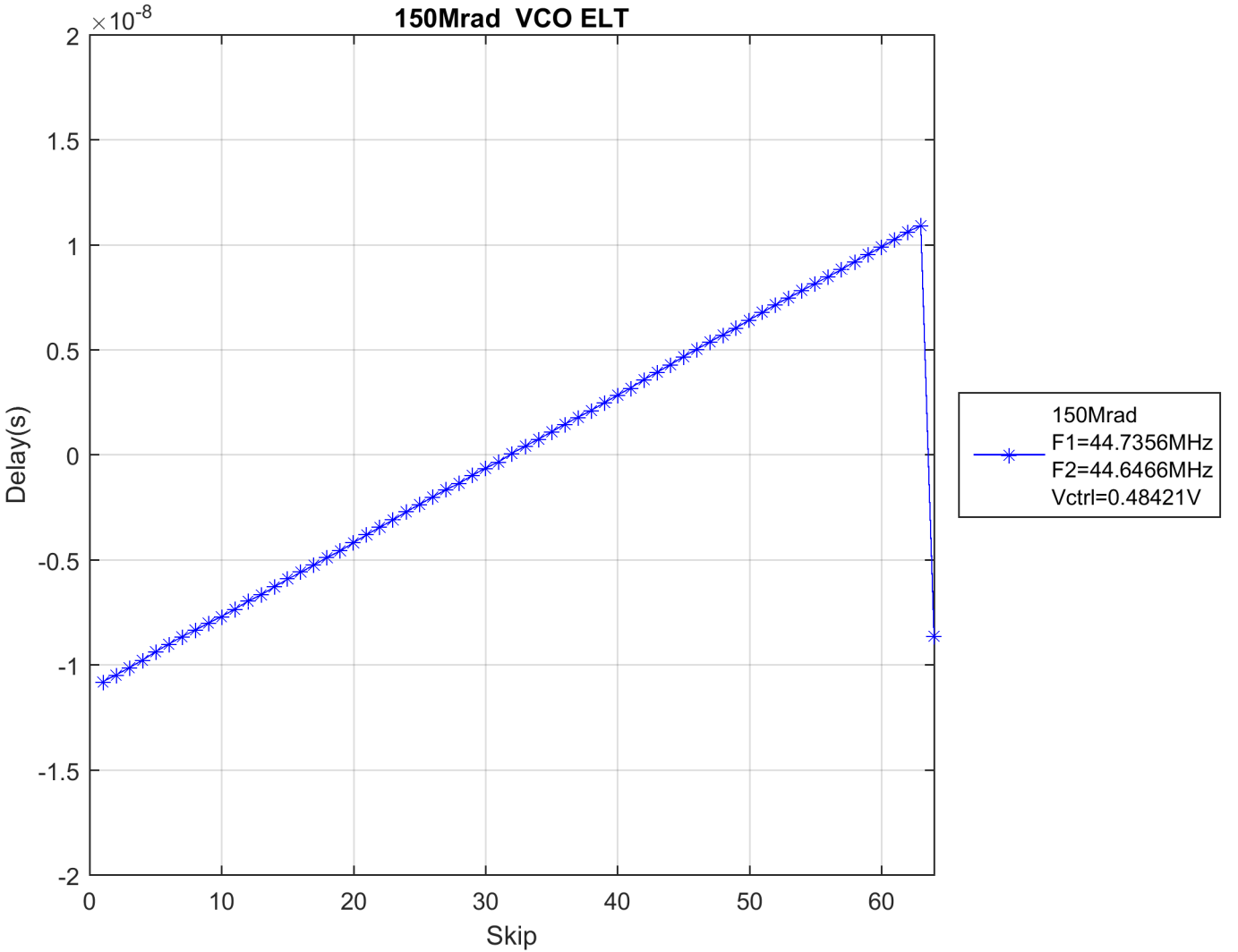

Pre-rad room T VCO ELT
×10-8
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
Delay(s)
0
10
20
30
40
50
60
Skip
Pre-rad room T
F1=47.203MHz
F2=47.1855MHz
Vctrl=0.48421V

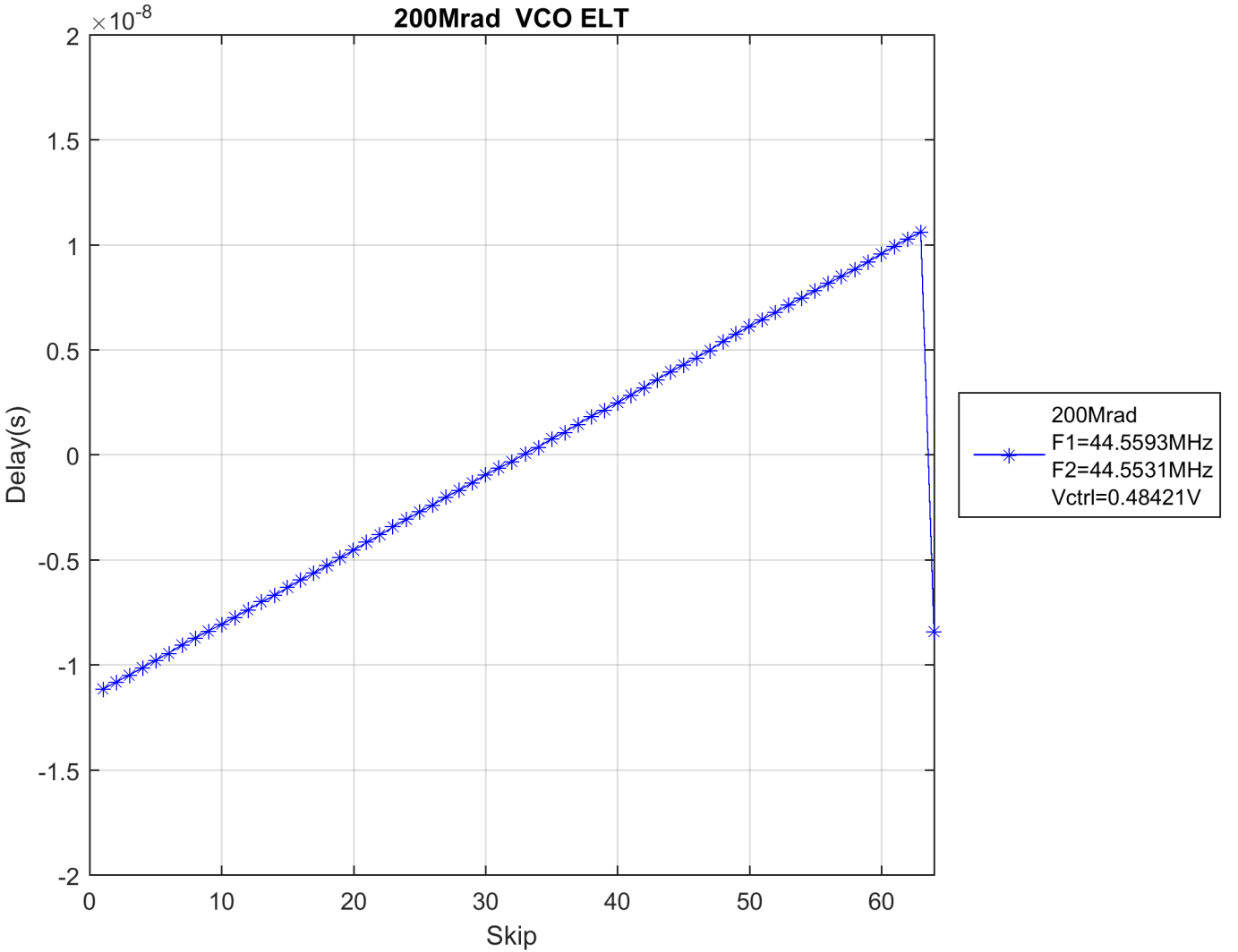

Pre-rad -20°C VCO ELT
×10-8
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
Delay(s)
0
10
20
30
40
50
60
Skip
Pre-rad -20°C
F1=44.7557MHz
F2=44.6543MHz
Vctrl=0.48421V

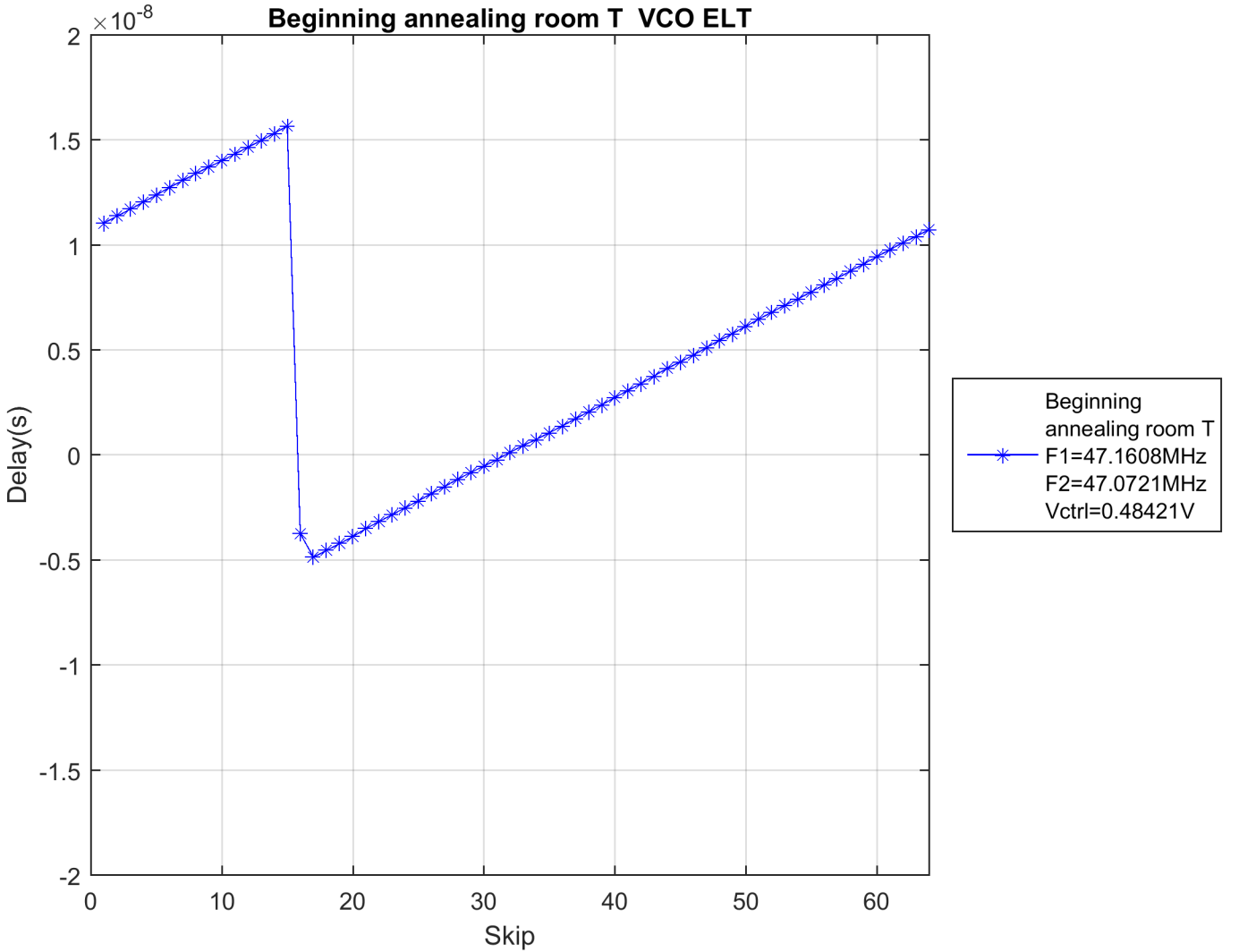

10Mrad VCO ELT
×10-8
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
Delay(s)
0
10
20
30
40
50
60
Skip
10Mrad
F1=45.0025MHz
F2=44.9636MHz
Vctrl=0.48421V

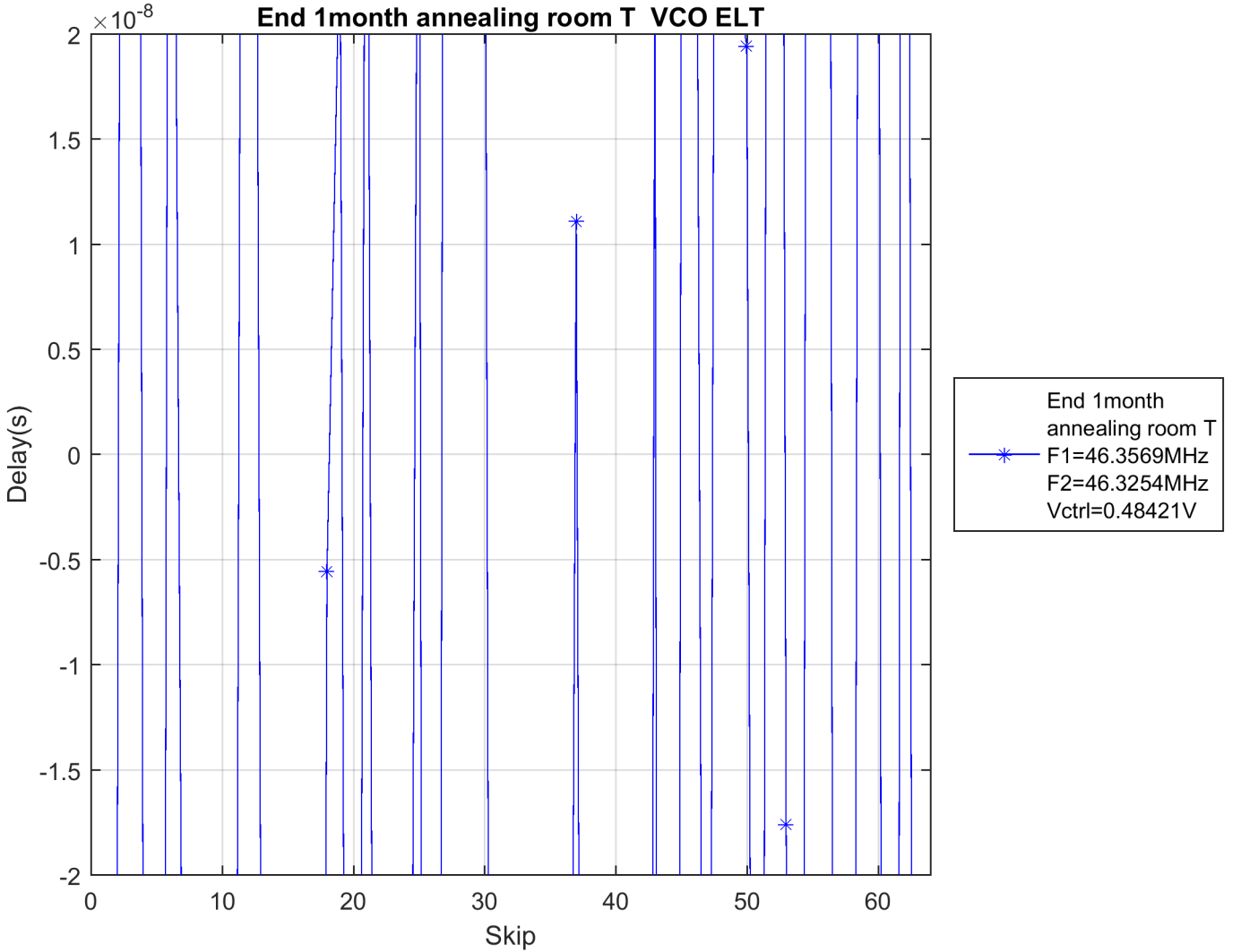

40Mrad VCO ELT
×10-8
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
Delay(s)
0
10
20
30
40
50
60
Skip
40Mrad
F1=44.99MHz
F2=44.9534MHz
Vctrl=0.48421V

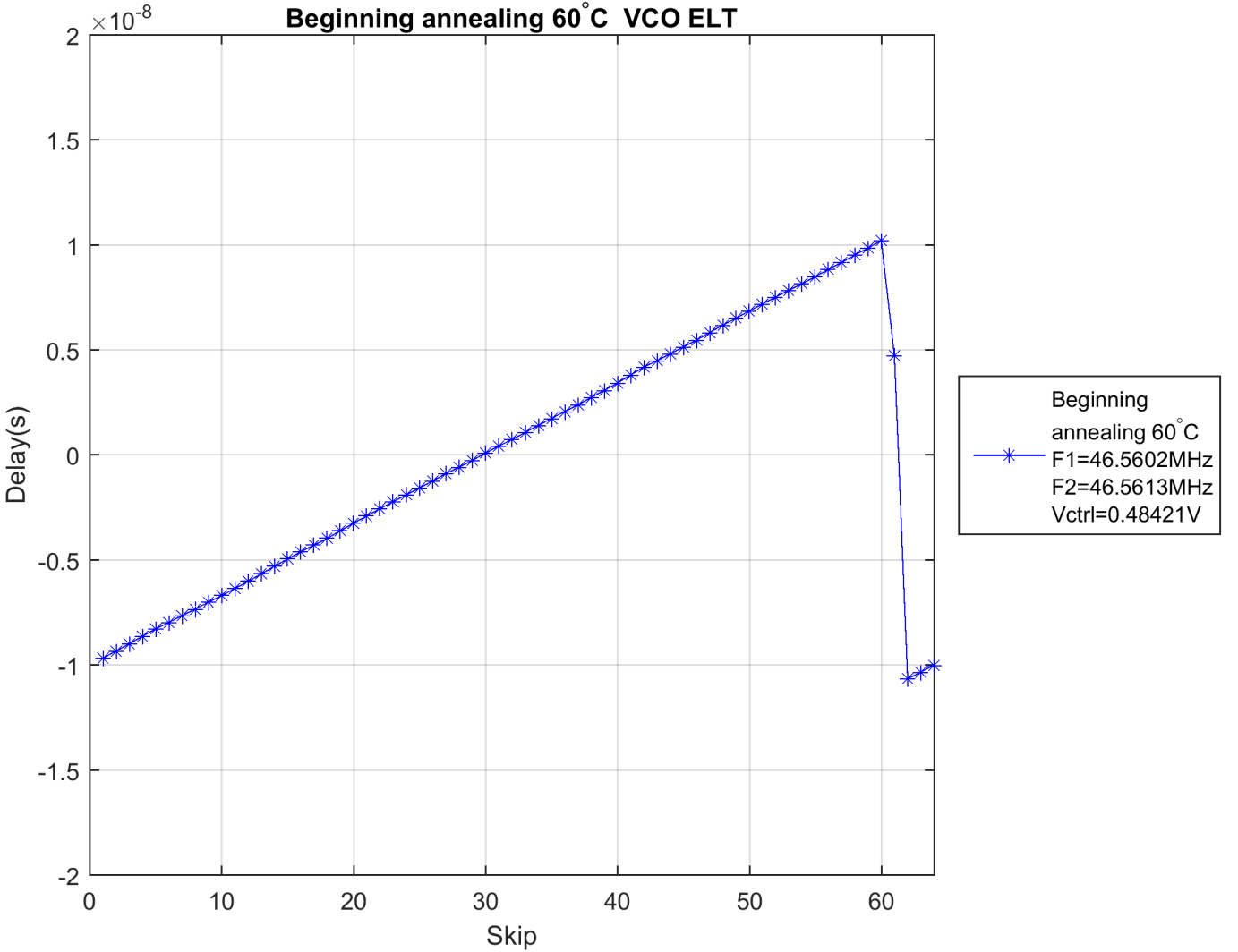

100Mrad VCO ELT
×10-8
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
Delay(s)
0
10
20
30
40
50
60
Skip
100Mrad
F1=44.922MHz
F2=44.8672MHz
Vctrl=0.48421V

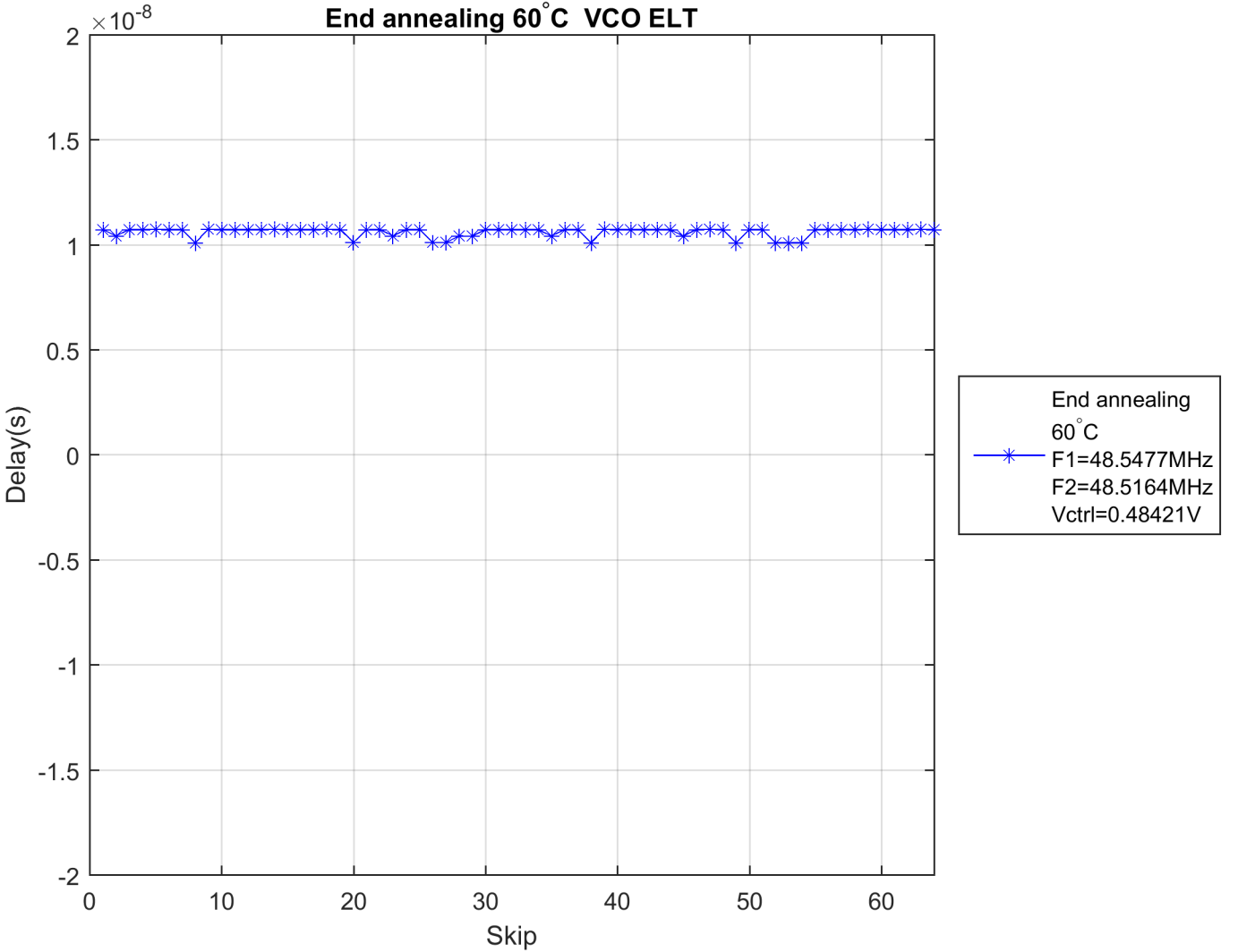

150Mrad VCO ELT
×10-8
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
Delay(s)
0
10
20
30
40
50
60
Skip
150Mrad
F1=44.7356MHz
F2=44.6466MHz
Vctrl=0.48421V

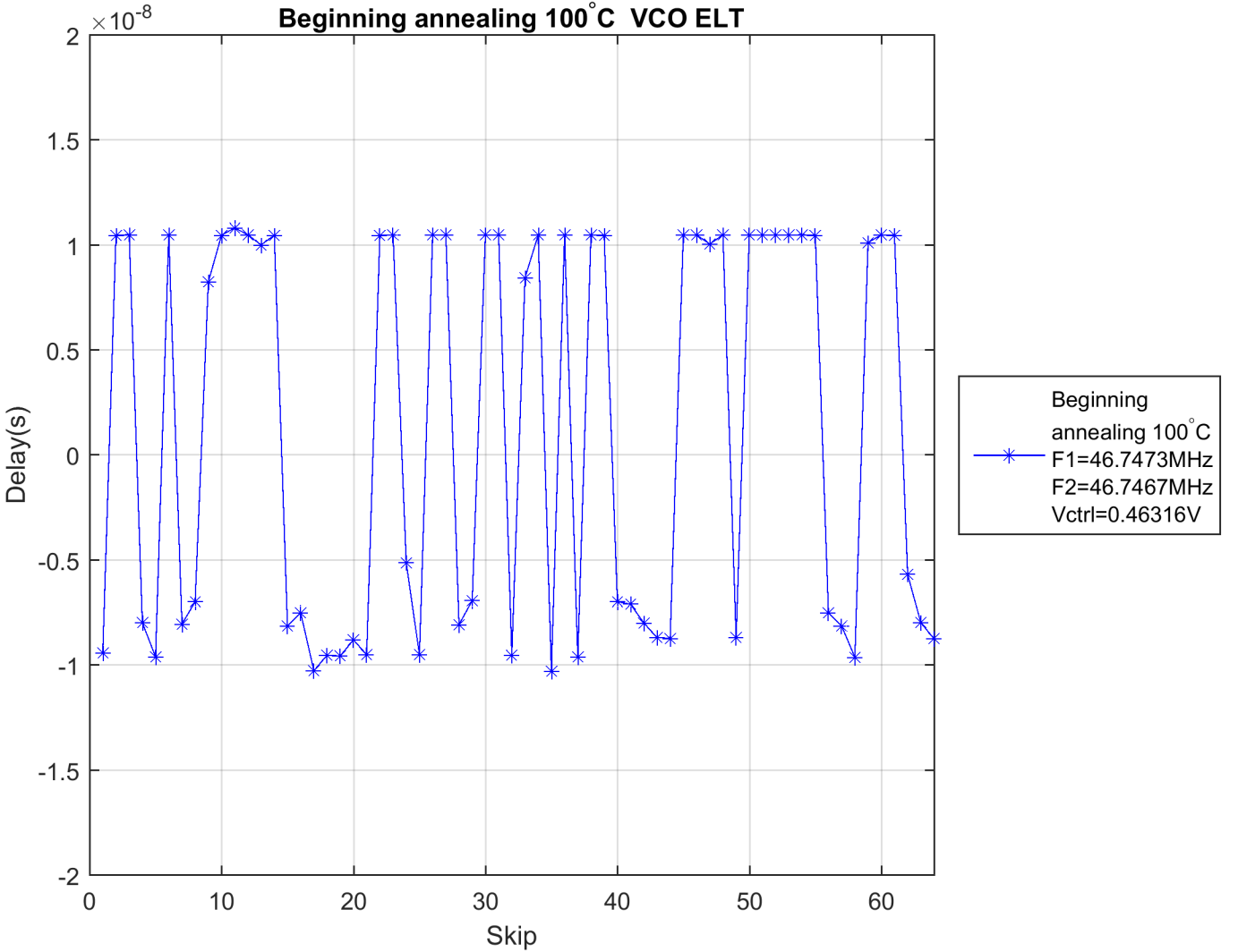

200Mrad VCO ELT
×10-8
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
Delay(s)
0
10
20
30
40
50
60
Skip
200Mrad
F1=44.5593MHz
F2=44.5531MHz
Vctrl=0.48421V

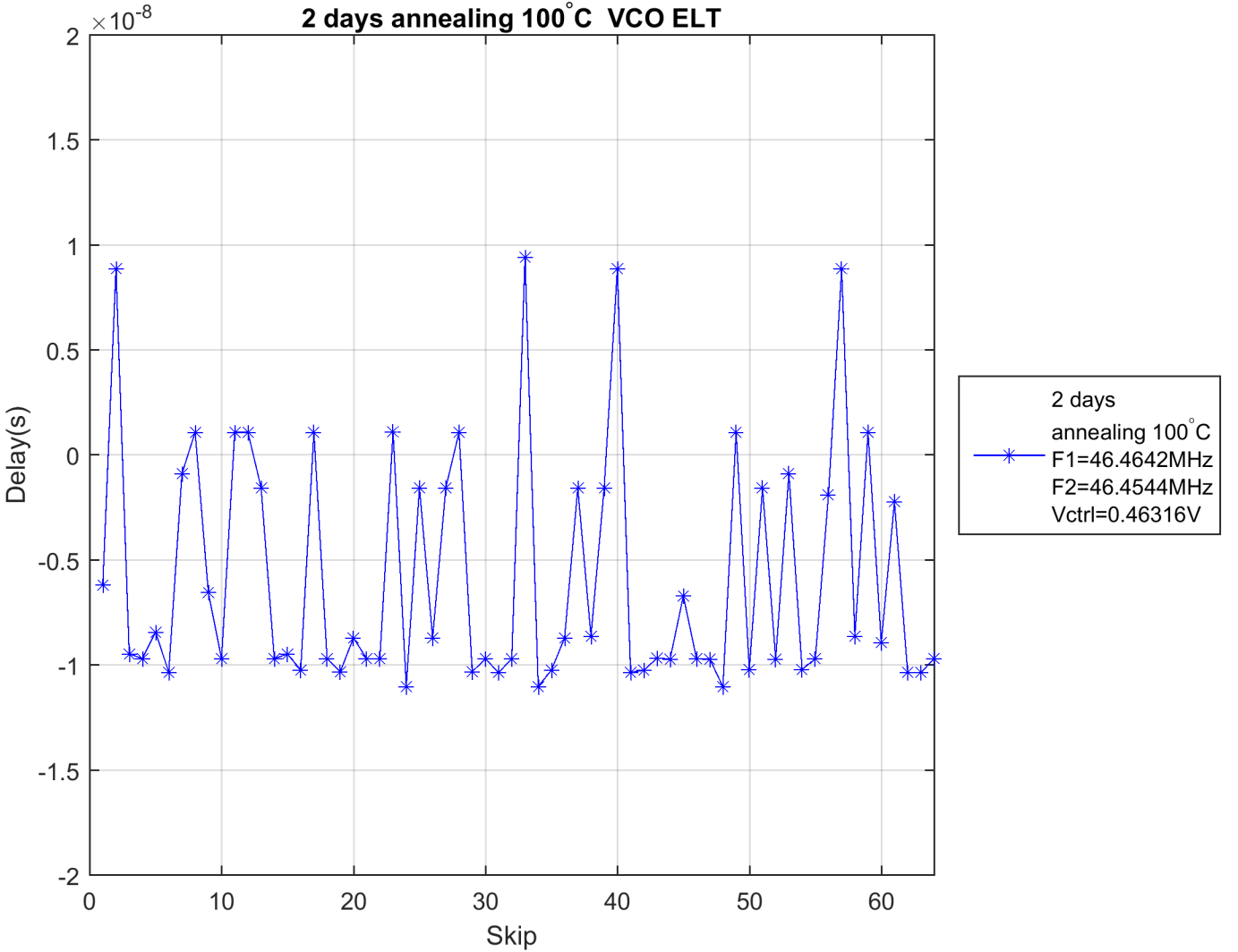

Beginning annealing room T VCO ELT
×10-8
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
Delay(s)
0
10
20
30
40
50
60
Skip
Beginning annealing room T
F1=47.1608MHz
F2=47.0721MHz
Vctrl=0.48421V


End 1month annealing room T VCO ELT
×10-8
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
Delay(s)
0
10
20
30
40
50
60
Skip
End 1month
annealing room T
F1=46.3569MHz
F2=46.3254MHz
Vctrl=0.48421V


Beginning annealing 60°C VCO ELT
×10-8
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
Delay(s)
0
10
20
30
40
50
60
Skip
Beginning annealing 60°C
F1=46.5602MHz
F2=46.5613MHz
Vctrl=0.48421V


End annealing 60°C VCO ELT
×10-8
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
Delay(s)
0
10
20
30
40
50
60
Skip
End annealing
60°C
F1=48.5477MHz
F2=48.5164MHz
Vctrl=0.48421V


Beginning annealing 100°C VCO ELT
×10-8
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
Delay(s)
0
10
20
30
40
50
60
Skip
Beginning annealing 100°C
F1=46.7473MHz
F2=46.7467MHz
Vctrl=0.46316V


2 days annealing 100°C VCO ELT
×10-8
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
Delay(s)
0
10
20
30
40
50
60
Skip
2 days
annealing 100°C
F1=46.4642MHz
F2=46.4544MHz
Vctrl=0.46316V